LittleBoard™ 550
Single Board Computer
Reference Manual

P/N 5001740A Revision A

Notice Page

REVISION HISTORY

Revision	Reason for Change	Date
A	Initial Release	Jan/05

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Audience Assumptions

This reference manual is for the person who designs computer related equipment, including but not limited to hardware and software design and implementation of the same. Ampro Computers, Inc. assumes you are qualified in designing and implementing your hardware designs and its related software into your prototype computer equipment.

Contents

List of Figures

List of Tables

Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the LittleBoard™ 550 single board computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- LittleBoard 550 Specifications
- Environmental requirements
- Major integrated circuits (chips) and features implemented
- LittleBoard 550 connector/pin numbers and definition
- BIOS Setup information

Information not provided in this reference manual includes:

- Detailed chip specifications
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry standard busses and signals

Reference Material

The following list of reference materials may be helpful for you to complete your design successfully. Most of this reference material is also available on the Ampro web site in the Embedded Design Resource Center. The Embedded Design Resource Center was created for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience.

Specifications

- PC/104 Spec Revision 2.5, November 2003
- PC/104-Plus Spec Revision 2, November 2003

  For latest revision of the PC/104 specifications, contact the PC/104 Consortium, at:

  Web site: http://www.pc104.org

- PCI 2.3 Compliant Specifications

  For latest revision of the PCI specifications, contact the PCI Special Interest Group Office at:

  Web site: http://www.pcisig.com

Chip (integrated circuits) specifications used on the LittleBoard 550:

- VIA Technologies, Inc. the Eden™ ESP processors, and the chips, VT8606 and VT82C686B, used for the Northbridge/Video controller and Southbridge respectively

  Web site: http://www.viatech.com

- Winbond Electronics, Corp. and the W83877TF chip used for the secondary I/O controller

  Web site: http://www.winbond-usa.com/products/winbond_products/pdfs/PCIC/877tf.pdf

- Intel Corporation and the chip, 82551ER, used for the Ethernet controllers

  Web site: http://developer.intel.com/design/network/products/82551er_DS

Related Ampro Products

The following items are directly related to successfully using the Ampro product you have just purchased or plan to purchase. Ampro highly recommends that you purchase and utilize a LittleBoard 550 QuickStart Kit or Development System.

LittleBoard 550 Support Products

- LittleBoard 550 QuickStart Kit (QSK)

  The QuickStart Kit includes the LittleBoard 550, RAM, an I/O interface board, a cable kit, documentation, and drivers for the unique devices used with Ampro supported operating systems.

- LittleBoard 550 Development System

  The Development System is a benchtop system, which provides a "known good" environment for your development work. The Development System provides an integrated and easy-to-use self-hosted development environment that lets you maximize the benefit of using an off-the-shelf board as the basis of your embedded system design. You can install ISA bus or PCI bus expansion boards on the Development System chassis. The Development System is arranged to make all the components of your system accessible. Refer to the LittleBoard 550 Development System Users Guide on the LittleBoard 550 Documentation and Support Software (Doc & SW) CD-ROM for more information.

- LittleBoard 550 Documentation and Support Software CD-ROM

  The LittleBoard 550 Documentation and Support Software (Doc & SW) CD-ROM is provided with the LittleBoard 550. The CD-ROM includes all of the LittleBoard 550 documentation in PDF format, including this reference manual, the LittleBoard 550 QuickStart Guide, the LittleBoard 550 Development System Users Guide, software utilities, board support packages, and drivers.

Other LittleBoard Products

- LittleBoard 700 – This EBX single board computer (SBC) is a highly integrated, high-performance, rugged, high quality system based on Intel's 933MHz Low Voltage Pentium® III, 650MHz Low Voltage Celeron®, or 400MHz Ultra Low Voltage Celeron processors. In addition to the standard LittleBoard features (EBX form factor, PC/104 & PC/104-Plus interfaces, +5 volt power, watchdog timer, serial console, etc.), the LittleBoard 700 supports up to four EIDE Ultra DMA 33/66/100 IDE drives including a CompactFlash™ socket, two floppy disk drives, one ECP/EPP parallel port, four RS232/422/485 serial ports, four USB V1.1 ports, two Ethernet ports, IrDA, AC'97 audio interface, and PS/2 keyboard & serial mouse. It also supports Ampro BIOS extensions for OEM boot customization, power management features, up to 1GB of SDRAM in an DIMM slot, up to 32MB UMA of AGP 4X video with built-in LVDS, CRT, and 36-bit TFT support.

- LittleBoard 800 – This EBX single board computer (SBC) is a highly integrated, high-performance, rugged, high quality system based on Intel's 1.4GHz Low Voltage Pentium M 738, 1.0GHz Low Voltage Celeron M, or 600MHz Ultra Low Voltage Celeron M CPUs. In addition to the standard LittleBoard features (EBX form factor, PC/104 & PC/104-Plus interfaces, +5 volt power, watchdog timer, serial console, etc.), the LittleBoard 800 supports up to four EIDE Ultra DMA 33/66/100 IDE drives including a CompactFlash socket, two floppy disk drives, one ECP/EPP parallel port, four RS232/422/485 serial ports, four USB 2.0 ports, two Ethernet ports (one Gigabit port), IrDA, AC'97 audio interface, and PS/2 keyboard & serial mouse. It also supports Ampro BIOS extensions for OEM boot customization, power management features, up to 1GB of DDR RAM in an DIMM slot, up to 64MB UMA of AGP 4X 128-bit 3D video interface with built-in dual channel LVDS and CRT support.

Other Ampro Products

- CoreModule™ Family – These complete embedded-PC subsystems on single PC/104 or PC/104-Plus form-factor (3.6x3.8 inches) modules feature 486, VIA Eden ESPs, Celeron®, or Celeron M CPUs. Each CoreModule includes a full complement of PC core logic functions, plus disk controllers, and serial and parallel ports. Most modules also include CRT and flat panel graphics controllers and/or an Ethernet interface. The CoreModules also come with built-in extras to meet the critical reliability requirements of embedded applications. These include onboard solid state disk compatibility, watchdog timer, smart power monitor, and Ampro embedded BIOS extensions.

- MiniModule™ Family – This extensive line of peripheral interface modules compliant with PC/104 and PC/104-Plus standards can be used with Ampro CoreModule, LittleBoard, and ReadyBoard single-board computers to configure embedded system solutions. Ampro's highly reliable MiniModule products currently support USB 2.0, IEEE 1394 (Firewire), Ethernet, PC Card expansion, analog/data acquisition, additional RS232/RS485 serial ports, and general-purpose I/O (GPIO).

- MightyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the Mini-ITX form factor (6.7" x 6.7") and are available with Intel® processors, including Pentium M. MightyBoard products offer the equivalent functions of a complete laptop or desktop PC system, including DDR memory, high performance graphics, USB 2.0, Gigabit Ethernet, plus standard PCI expansion capability in one card slot. Ampro includes configuration control and embedded BIOS extension such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

- ReadyBoard™ Family – These low-cost, high-performance single-board computers (SBC) use the EPIC form factor (4.5”x6.5”) and are available with the VIA Eden™, Intel Pentium® III, Celeron®, Pentium M and Celeron M processors. ReadyBoard products offer functions equivalent to a complete laptop or desktop PC system, plus several expansion cards. Ampro includes configuration control and embedded BIOS extension such as watchdog timer, battery-free boot, a customizable splash screen, BIOS recovery, and serial console.

- ETX Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various x86 processors from 300MHz VIA Eden ESP to 1.4GHz Low Voltage Pentium M 738 CPUs in an ETX Revision 2.6 form factor to plug into your custom baseboard. Each ETX module provides standard peripherals, including dual Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, ISA bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, USB ports, Video, and AC’97 sound. ETX modules support up to 512MB or more of SODIMM DRAM. Optional –40°C to +85°C operation, along with a 50% thicker PCB are available to meet your rugged application requirements.

- EnCore™ Family – These high-performance, compact, rugged Computer-on-Module (COM) solutions use various processor technologies including x86, MIPS®, and PowerPC™ architectures to plug into your custom baseboard. Each EnCore module provides standard peripherals, including Ultra/DMA 33/66/100 IDE, floppy drive interface, PCI bus, serial, parallel, PS/2 keyboard and mouse interfaces, 10/100BaseT Ethernet, and USB ports. Some EnCore modules also provide video and AC'97 sound. Depending on the model, EnCore modules support up to 256MB or 512MB of SODIMM DRAM. Extended temperature support up to +85°C is available.

Chapter 2 Product Overview

This introduction presents general information about the EBX Architecture and the LittleBoard 550 single board computer (SBC). After reading this chapter you should understand:

- EBX Architecture
- LittleBoard 550 architecture
- LittleBoard 550 features
- Major components
- Connectors
- Specifications

EBX Architecture

The "Embedded Board, eXpandable" (EBX) standard is the result of a collaboration between industry leaders, Motorola and Ampro, to unify the embedded computing industry on a small footprint embedded single-board computer (SBC) standard. The EBX standard principally defines physical size, mounting hole pattern, and power connector locations. It does not specify processor type or electrical characteristics. There are recommended connector placements for serial/parallel, Ethernet, graphics, and memory expansion, including an optional location for PC Card (PCMCIA) expansion.

Derived from the Ampro LittleBoard™ form-factor originated in 1984, EBX combines a standard footprint with open interfaces. The EBX form-factor is small enough for deeply embedded applications, yet large enough to contain the functions of a full embedded SBC (single board computer) including CPU, memory, mass storage interfaces, display controller, serial/parallel ports, today's advanced operating systems, and other system functions. This embedded SBC standard ensures that embedded system OEMs can standardize their designs and that embedded computing solutions can be designed into space constrained environments with off-the-shelf components.

The EBX standard boasts highly flexible and adaptable system expansion, allowing easy and modular addition of functions such as USB 2.0, Firewire or wireless networking not usually contained in standard product offerings. The EBX system expansion is based on popular existing industry standards, PC/104™ and PC/104-*Plus*™. PC/104 places the ISA bus on compact 3.6" x 3.8" modules with self-stacking capability. PC/104-*Plus* adds the power of a PCI bus to PC/104 while retaining the basic form-factor. Using PC/104 expansion cards, the PCMCIA standard offers access to PC Cards from the mobile and handheld computing markets.

The EBX standard integrates all these off-the-shelf standards into a highly embeddable SBC form-factor. EBX supports the legacy of PC/104, hosting the wide variety of embedded system oriented expansion modules from hundreds of companies worldwide. PCMCIA brings the advantages of the latest portable and mobile system expansion technologies to embedded applications. Additionally, the EBX PCI infrastructure and PC/104-*Plus* expansion bus offer true processor independence and high performance standards-based system expansion. See Figure 2-1.

The EBX standard also brings stability to the embedded board market and offers OEMs assurance that a wide range of products will be available from multiple sources – now and in the future. The EBX standard is open to continuing technology advancements, since it is both processor and payload independent. It creates opportunity for economies of scale in chassis, power supply, and peripheral devices.

The EBX specification is freely available to all interested companies, and may be used without licenses or royalties. For further technical information on the EBX standard, go to the Ampro web site at www.ampro.com, or to the PC/104 Consortium web site at www.pc104.org.

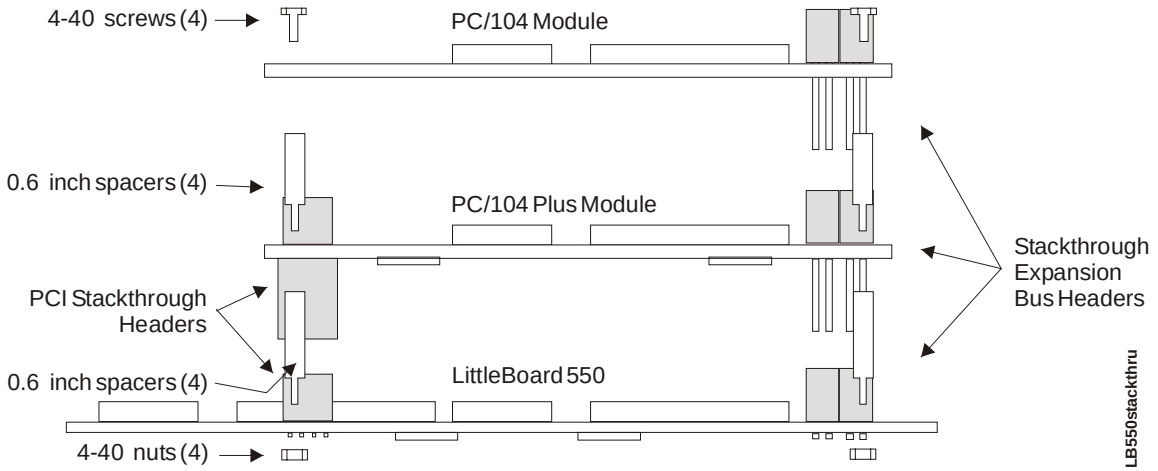


Figure 2-1. Stacking PC/104 Modules with the LittleBoard 550

Product Description

The LittleBoard 550 is an exceptionally high integration, high performance, rugged, and high quality single-board system, which contains all the component subsystems of a PC/AT PCI motherboard plus the equivalent of up to 5 PCI expansion boards. The LittleBoard 550 is based on one of these ultra high performance, high-integration processors; 1GHz Via 1Eden™ ESP 10000, 533MHz Eden™ ESP 5000, or the low cost 300MHz Eden™ ESP 3000 CPU. This gives designers more of a choice when selecting a complete, high performance embedded processor based on the EBX form factor that conforms to the EBX V1.1 specifications.

Each LittleBoard 550 incorporates the Via Technologies Twister-T chipset (VT8606 and VT82C686B) and a Secondary I/O controller in the Standard Microsystems, Super I/O (SP37E760) controller chip to provide a floppy and two Ultra/DMA 33/66/100 IDE controllers supporting two IDE drives each channel, four serial ports, a EPP/ECP parallel port, four USB OHCI ports, PS/2 keyboard and mouse interfaces, and an audio AC'97 CODEC on the board. The LittleBoard 550 also supports two independent 10/100BaseT interfaces, up to 1GB of SDRAM in a single 168-pin DIMM slot, and a AGP4x graphics controller, which provides CRT and flat panel video interfaces for the most popular LVDS and TFT/LCD panels.

The LittleBoard 550 can be expanded through the PC/104 and PC/104-Plus expansion buses for additional system functions. These busses offer compact, self-stacking, modular expandability. The PC/104 is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-Plus bus includes this signal set, and in addition, signals implementing a PCI bus, available on an additional 120-pin (4 rows of 30 pins) PCI expansion bus connector. The PCI bus operates at clock speeds up to 33MHz.

Among the many embedded-PC enhancements on the LittleBoard 550 that ensure embedded system operation and application versatility are a watchdog timer, serial console support, battery-free boot, on-board high-density CompactFlash socket, and BIOS extensions for OEM boot customization.

The LittleBoard 550 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with Ampro MiniModules™ or other PC/104-compliant expansion boards, or it can be used as powerful computing engine. The LittleBoard 550 requires a single +5V power supply.

Board Features

- CPU features
  - Via Eden™ ESP 10000 (1GHz), Eden ESP 5000 (533MHz) or Eden ESP 3000 (300MHz)
  - Each CPU has a Front Side Bus (FSB) of 133MHz, 133MHz, or 66MHz, respectively
- Memory
  - Provides a single standard 168-pin DIMM slot
  - Supports +3.3V SDRAM up to 1GB
  - Supports 133MHz (7.5ns) clock speed for Eden ESP 10000 and Eden ESP 5000
  - Supports 66MHz (15ns) clock speed for Eden ESP 3000
  - Serial EEPROM (SEEP)
    - 4k-bit Serial EEPROM
    - Supports 2-wire SMBus interface
    - Stores system Setup parameters and manufacturing information
    - Supports battery-free boot capability
    - 512 bits are available for OEM use
- PC/104 and PC/104-Plus Bus Interface
  - PC/104 Bus speed at 8MHz
  - PCI 2.3 compliant
  - PCI Bus speed at 33MHz
- IDE Interfaces
  - Supports two enhanced IDE controllers (4 devices)
  - Supports dual bus master mode
  - Supports Ultra DMA 33/66/100 modes
  - Supports ATAPI and DVD peripherals
  - Supports IDE native and ATA compatibility modes
  - CompactFlash Adapter
    - Supports Type I or Type II PC Card socket
    - Supports IDE CompactFlash Card
    - Supports primary IDE bus with Master/Slave jumper
    - Supports bootable CompactFlash
- Floppy Disk Interface
  - Supports two floppy drives
  - Supports all standard PC/AT formats: 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB
- Serial Ports
  - Four buffered serial ports with full handshaking
  - Provides 16550-equivalent controllers, each with a built-in 16-byte FIFO buffer
  - Supports full modem capability on two of the four ports

- Supports RS232, RS485, or RS422 operation on each port
- Supports programmable word length, stop bits, and parity
- Supports 16-bit programmable baud-rate generator and a interrupt generator.

- Parallel Port
  - Supports standard printer port
  - Supports IEEE standard 1284 protocols of EPP and ECP outputs
  - Bi-directional data lines
  - Supports 16 byte FIFO for ECP mode.
- USB Ports
  - Supports two root USB hubs
  - Supports up to four USB ports
  - Supports USB bootable devices
  - Supports USB v1.1 and Universal OHCI v1.1
  - Supports over-current fuses on board
  - Supports over-current detection status on board
- Keyboard/Mouse Interface
  - Supports PS/2 keyboard
  - Supports PS/2 mouse
- Audio interface
  - Supports AC'97 standard
  - AC'97 CODEC on board
  - Audio amplifier on board
- Ethernet Interface
  - Supports two fully independent Ethernet ports
  - Integrated LEDs on each port (Link/Activity and Speed)
  - Two Intel 82551ER Controller chips
  - Supports IEEE 802.3 10BaseT/100BaseTX compatible physical layer
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhance proprietary collision reduction mode

- Video Interfaces (CRT/LVDS)
  - Supports CRT (1600 x 1200) with 32MB SMA (Shared Memory Area)
  - AGP 4X graphics
  - Compliant with Rev 2.0 of AGP Interface
  - 36-bit flat panel outputs (DSTN, TFT)
  - LVDS outputs (1 or 2 channel, four differential signals 3-bits + clock)
- Miscellaneous
  - Real-time clock (RTC) operation on board
  - Battery-free boot
  - Provides battery socket for Lithium Battery
  - Supports external battery connection
  - Thermal and Voltage monitoring
  - Oops! Jumper (BIOS recovery) support
  - USB boot
  - LAN Boot (optional, requires BIOS upgrade)
  - Serial Console support
  - Watchdog timer

Block Diagram

Figure 2-3 shows the functional components of the board.

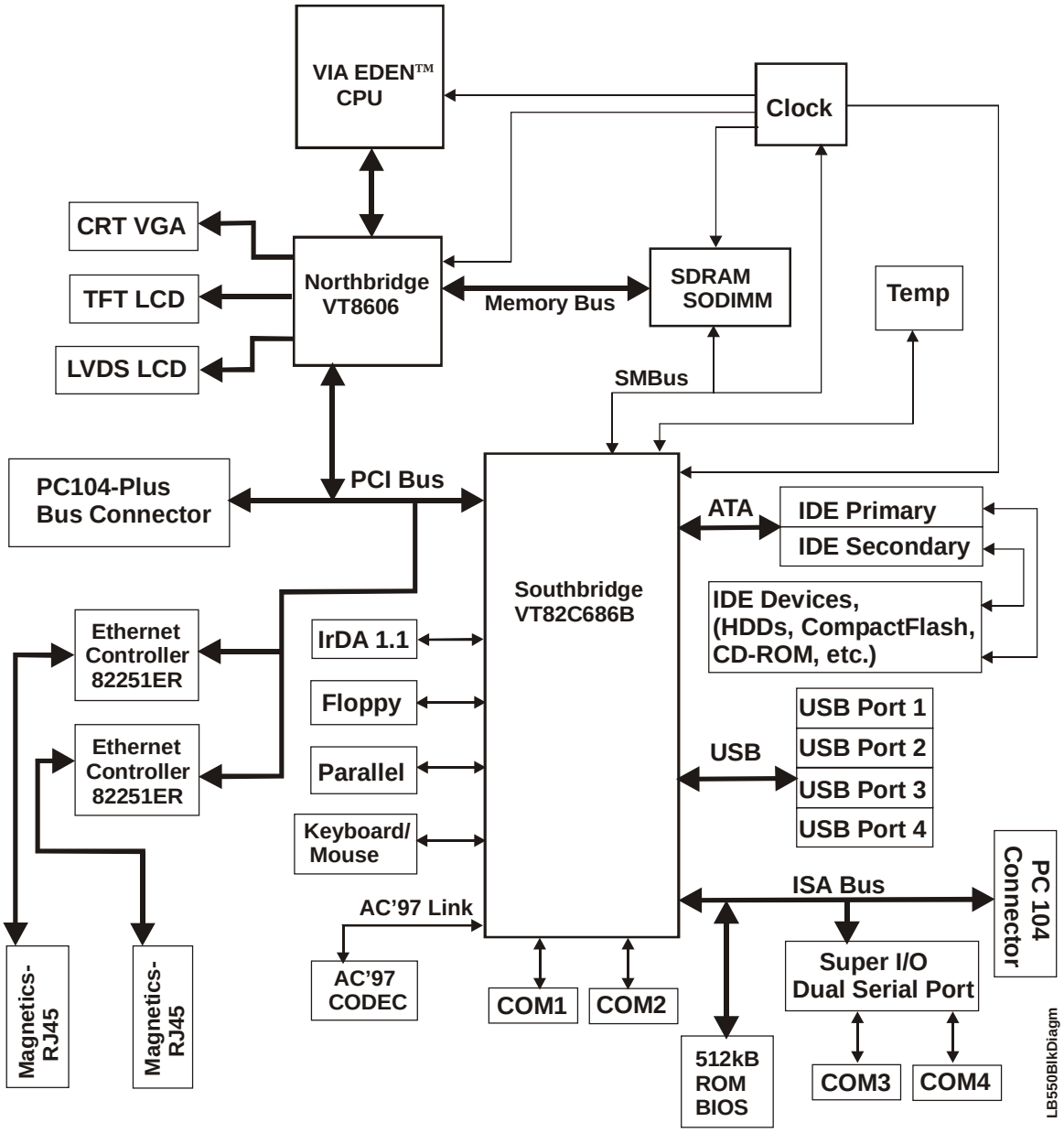


Figure 2-2. LittleBoard 550 Functional Block Diagram

Major Integrated Circuits (ICs)

Table 2-1 lists the major integrated circuits, including a brief description of each, on the LittleBoard 550 and Figure 2-4 shows the location of the major chips.

Table 2-1. Major Integrated Circuit Description and Function

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	VIA Technologies, Inc.	Eden ESP 10000, ESP 5000, ESP 3000	CPUs offered at 1GHz, 533MHz, and 300MHz	Embedded CPU
Northbridge (U2)	VIA Technologies, Inc.	VT8606 (Twister-T)	Northbridge functions plus Video	Memory and Video
Southbridge (U3)	VIA Technologies, Inc.	VT82C686B	Southbridge provides most standard I/O functions	I/O Functions
Super I/O (U13)	Standard Microsystems	SP37E760	This Super I/O controller provides two additional serial ports	Serial ports
Ethernet Controllers (U5, U6)	Intel	82551ER	Ethernet Controllers provided by two independent 10/100BaseT Ethernet.	Ethernet functions

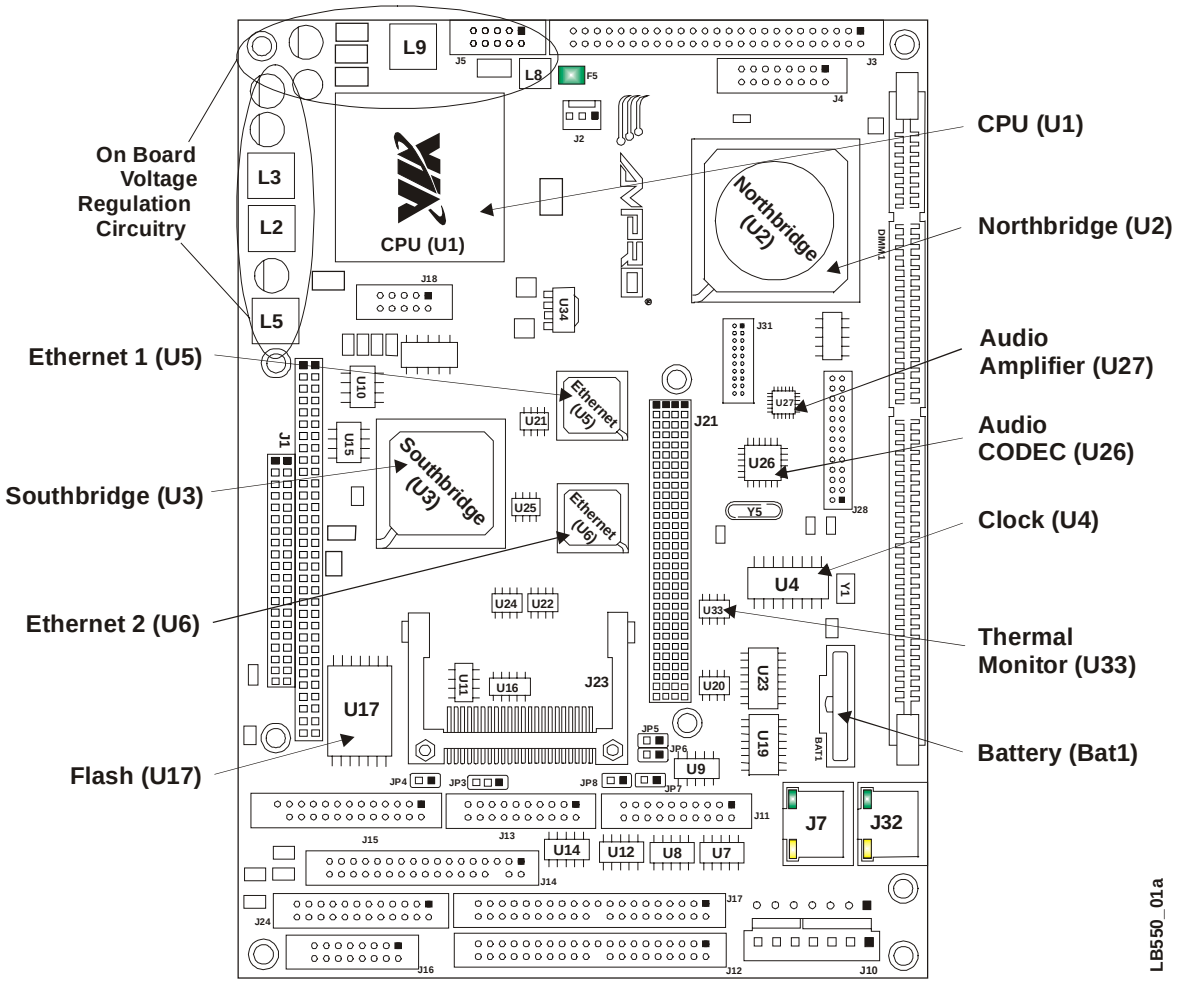


Figure 2-3. LittleBoard 550 Component Location (Top view)

Connector Definitions

Table 2-2 describes the connectors shown in Figures 2-3 to 2-5. All I/O connectors use 0.1" pin spacing unless otherwise indicated.

Table 2-2. Connector Descriptions

Jack #	Signal	Description
J1A/J1B & J1C, J1D	PC/104 bus	104-pins for PC/104 connector
J2	Fan connector	3-pin header provides +5v and ground to fan.
J3	Video (LCD 1)	50-pin connector part of video output for LCD panels (lower 24-bits)
J4	Video (LCD 2)	16-pin connector part of video output for LCD panels (upper 12 bits)
J5	Video (CRT)	10-pin connector for output to a CRT type monitor
J7	Ethernet 1	8-pin RJ45 connector for Ethernet port 1
J8	Ethernet 1	Optional 6-pin header for Ethernet port 1; for special builds only
J9	Ethernet 2	Optional 6-pin header for Ethernet port 2, for special builds only
J10	Power In	7-pin connector for input power
J11	Serial A	20-pin connector for serial ports 1 and 2
J12	Primary IDE	40-pin connector for the primary IDE interface
J13	Serial B	20-pin connector for serial ports 3 and 4
J14	Floppy	34-pin connector for floppy disk drive interface
J15	Parallel	26-pin connector for parallel interface
J16	Utility 1	16-pin connector for keyboard, external battery, reset switch, speaker
J17	Secondary IDE	40-pin connector for the secondary IDE interface
J18	Utility 3	10-pin connector provides USB2 and USB3 output
J21	PC/104-Plus	120-pin, 2mm, connector for PCI bus
J23	CompactFlash	50-pin socket accepts Type 1 or Type II CompactFlash cards
J24	Utility 2	24-pin connector for mouse, SMBus, USB 0 & 1, power button
J28	Audio In/Out	26-pin, 2mm, connector for all of the Audio signals (input/output)
J31	Video (LVDS)	20-pin, 1.25mm, connector for LVDS type video displays
J32	Ethernet 2	8-pin RJ45 connector for Ethernet port 2
DIMM1	Memory	168-pin socket for SDRAM DIMMs

Additional Components

The fuses in Table 2-3 are shown in Figures 2-4 and 2-6.

Table 2-3. Additional Component Descriptions

Component	Description
F1 (1.5A) Auto Reset	Overcurrent Fuse for USB0 on connector J24
F2 (1.5A) Auto Reset	Overcurrent Fuse for USB1 on connector J24
F3 (1.5A) Auto Reset	Overcurrent Fuse for USB2 on connector J18
F4 (1.5A) Auto Reset	Overcurrent Fuse for USB3 on connector J18
F5 (1.5A) Auto Reset	Fuse for the CRT on connector J5

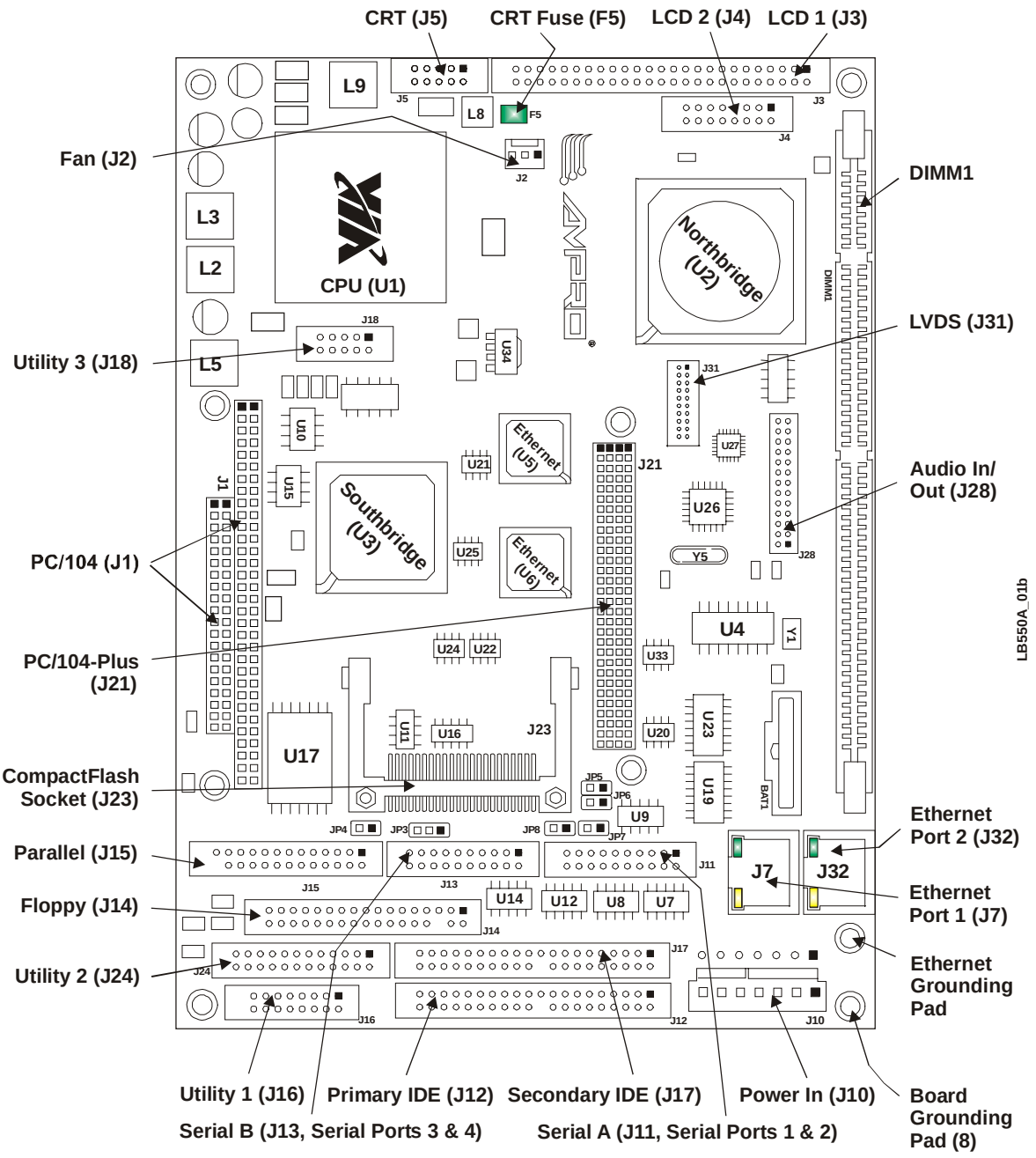


Figure 2-4. Connector and Fuse Locations (Top view)

CAUTION	The two Ethernet ports share a common ground (transformer center tap), that is floating until you determine how the common ground is connected. The grounding holes (8) of the LittleBoard 550 are connected to ground potential (return) of the DC power supply connected to the board through J10.

NOTE	Pin-1 is shown as a black pin (square or round) in all connectors and jumpers in all illustrations.

Jumper Definitions

Table 2-4 describes the jumpers shown in Figure 2-5.

Table 2-4. Jumper Settings

Jumper #	Installed	Removed/Installed
JP3 – CompactFlash Voltage Select	Enable +5V (1-2) (**Default**)	Enable +3.3V (1-3)
JP4 – CompactFlash Master/Slave Select	Enable Master (pins 1-2)	Enable Slave (Removed) (**Default**)
JP5 – Serial Port 1 (COM1) RS485 Termination	Enable Termination (1-2)	Disable Termination (Removed) (**Default**)
JP6 – Serial Port 2 (COM2) RS485 Termination	Enable Termination (1-2)	Disable Termination (Removed) (**Default**)
JP7 – Serial Port 3 (COM3) RS485 Termination	Enable Termination (1-2)	Disable Termination (Removed) (**Default**)
JP8 – Serial Port 4 (COM4) RS485 Termination	Enable Termination (1-2)	Disable Termination (Removed) (**Default**)

LED Definitions

Tables 2-5 and 2-6 provide the LED colors and definitions for the Ethernet ports, Port 1 (J7) and Port 2 (J32) located on the LittleBoard 550. Refer to Figure 2-5.

Table 2-5. Ethernet Port 1 (J7) LED Indicators

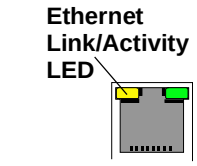
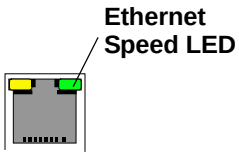
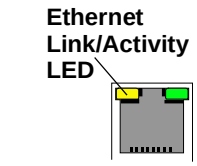
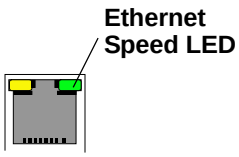
Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 1 (J7). • A **steady On** LED indicates a link is established • A **flashing** LED indicates active data transfers
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 1 (J7). • A steady **Off** LED shows the port at 10BaseT speed • A steady **On** LED shows the port at 100BaseT speed

Table 2-6. Ethernet Port 2 (J32) LED Indicators

Indicator	Definition
	Link/Activity LED – This yellow LED is the activity/link indicator and provides the status of Ethernet port 2 (J32). • A **steady On** LED indicates a link is established • A **flashing** LED indicates active data transfers
	Speed LED – This green LED is the Speed indictor and indicates transmit or receive speed of Ethernet port 2 (J32). • A steady **Off** LED shows the port at 10BaseT speed • A steady **On** LED shows the port at 100BaseT speed

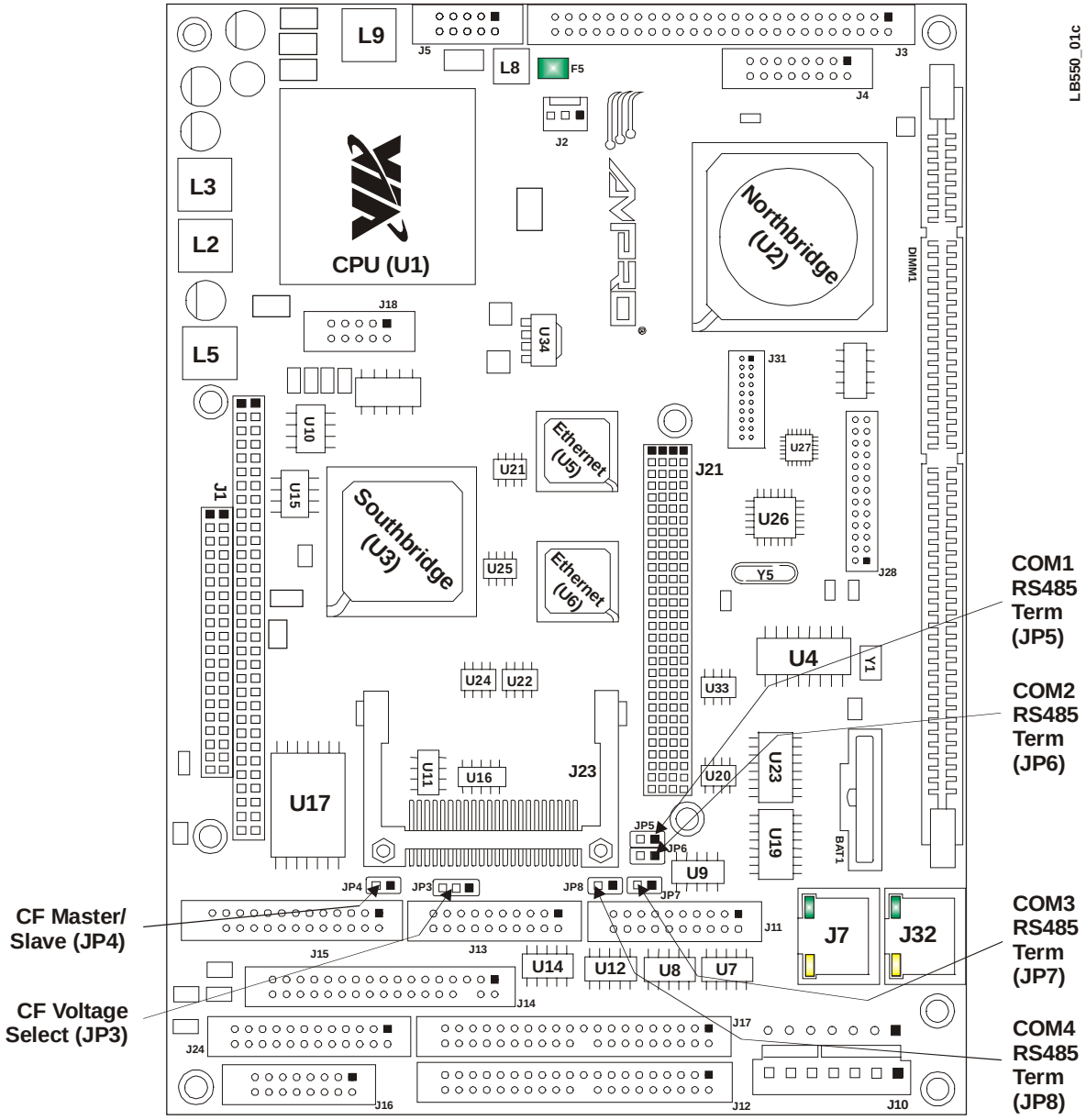


Figure 2-5. Jumpers Locations (Top view)

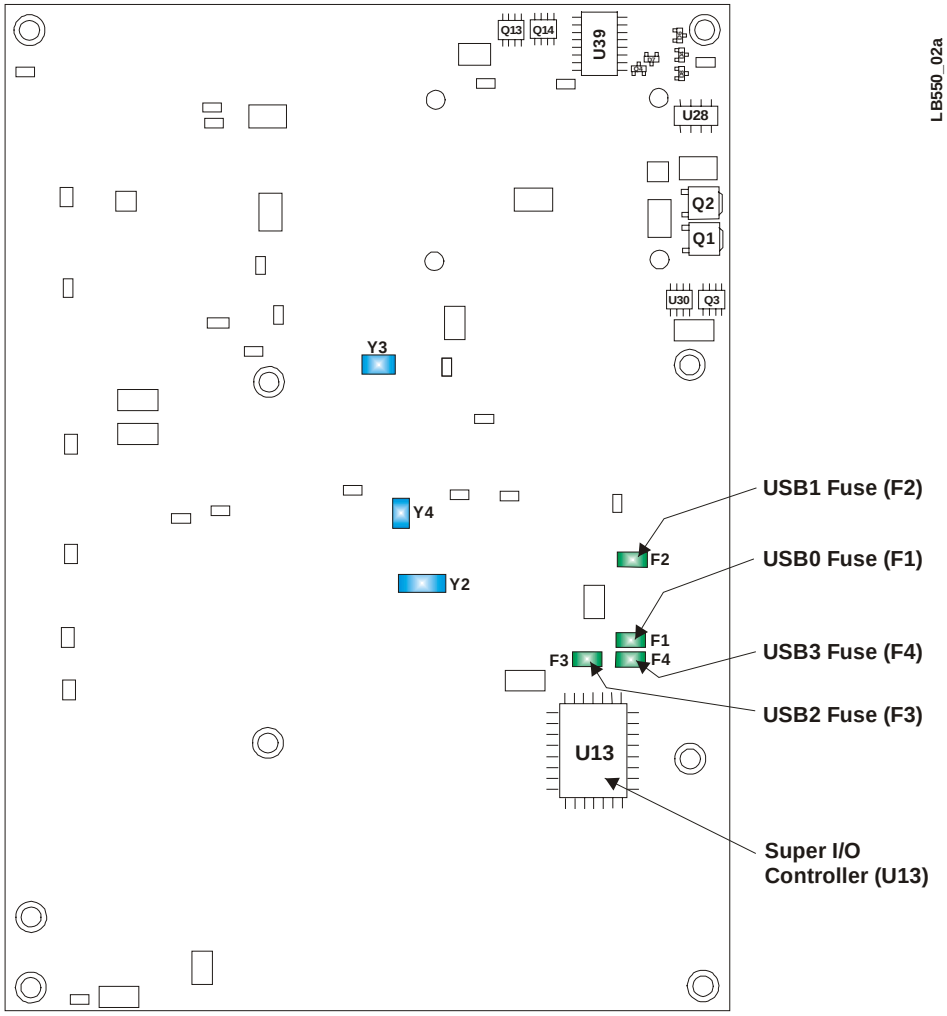


Figure 2-6. Component and Fuses Locations (Bottom view)

Specifications

Physical Specifications

Table 2-7 gives the physical dimensions of the board and Figures 2-7 and 2-8 give the mounting dimensions and pin-1 connector locations.

Table 2-7. Weight and Footprint Dimensions

Item	Dimension
Weight	0.323kg. (0.712lbs.)
Height (overall)	25.37mm (0.999”)
Width	146mm (5.75”)
Length	203mm (8.0”)
Thickness	2.36mm (0.093”)

NOTE Overall height is measured from the upper board surface to the highest permanent component (battery in socket) on the upper board surface. This measurement does not include the various heatsinks for the CPUs or DIMM sizes inserted into the socket. The heatsinks or DIMMs could increase this dimension.

Mechanical Specifications

Figures 2-7 and 2-8 show top views of the LittleBoard 550 with the mechanical mounting dimensions.

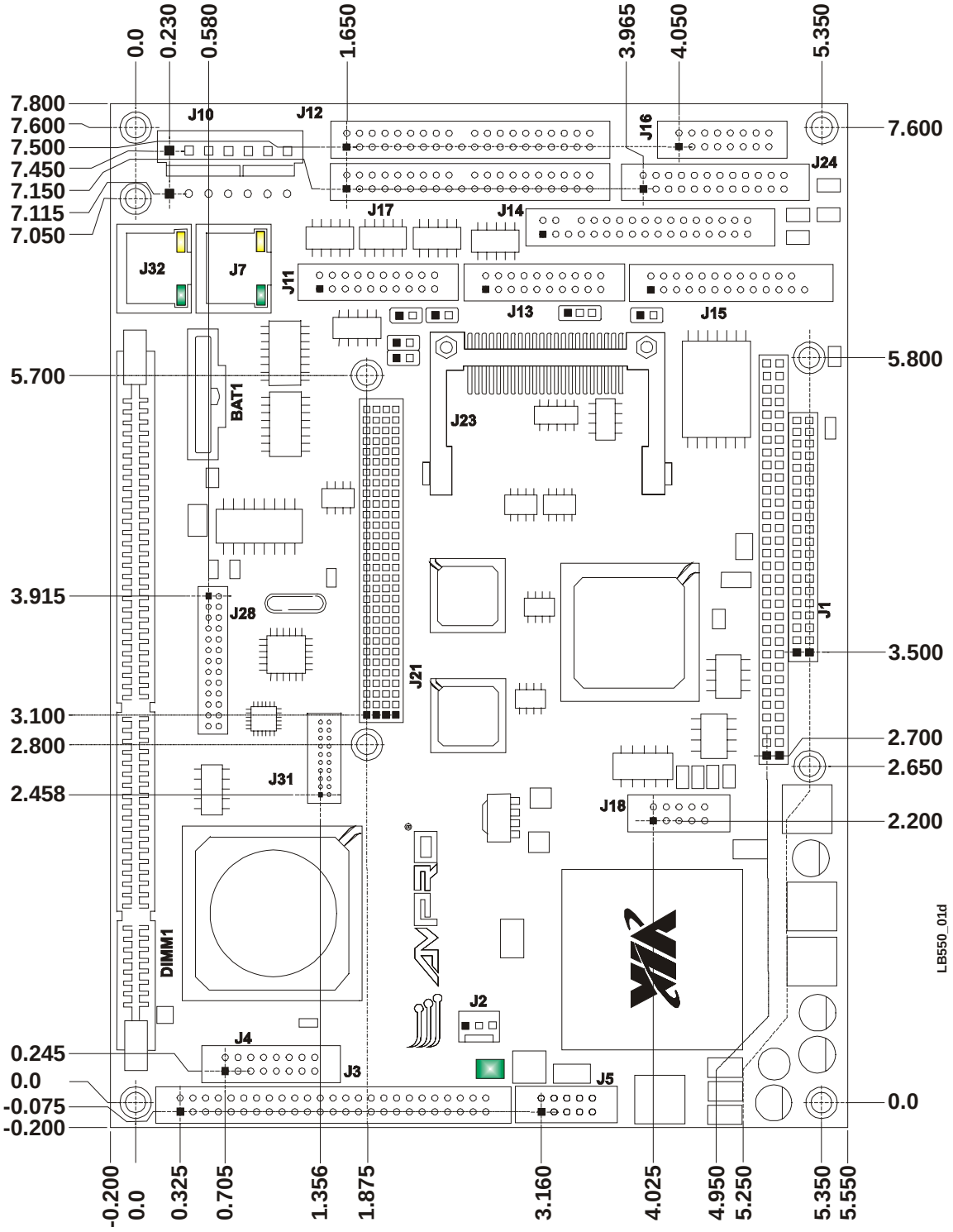


Figure 2-7. LittleBoard 550 Dimensions (Top view, #1)

NOTE	All dimensions are given in inches.

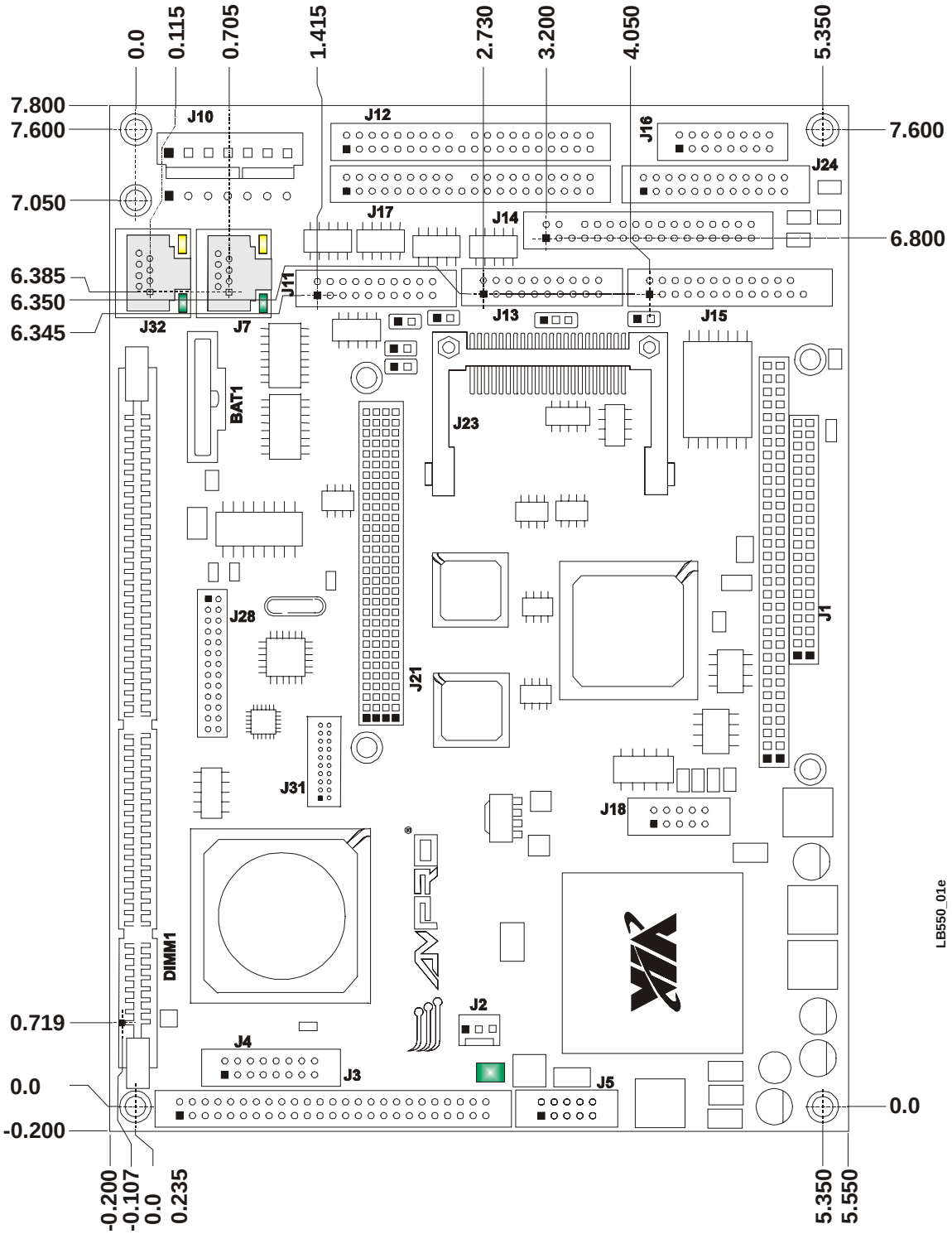


Figure 2-8. LittleBoard 550 Dimensions (Top view, #2)

NOTE	All dimensions are given in inches.

Power Specifications

Table 2-8 shows the power requirements for the LittleBoard, including the I/O interface board.

Table 2-8. Power Supply Requirements

Parameter	300MHz Characteristics	533MHz Characteristics	1GHz Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages	Regulated DC voltages
In-rush* Current (Typical)	26.9Amps (134.5W)	20.6Amps (103W)	25.9Amps (129.5W)
BIT** Current (Typical)	1.98Amps (9.92W)	2.51Amps (12.55W)	2.84Amps (14.21W)

Notes: *In-rush measured with video, 64MB memory, and power connected. **The BIT (burn in test) current was derived with 64MB SDRAM, (1) floppy, (1) IDE HDD, (1) on-board 64MB CompactFlash, I/O Interface board, (2) serial ports w/loopbacks, (1) externally-powered USB CD-ROM, (1) externally-powered USB HDD, (1) external USB Jump-drive (key-chain CompactFlash type), (1) external USB CompactFlash Reader with 64MB CompactFlash card, and (2) Ethernet channel connections using Win2k OS.

Environmental Specifications

Table 2-9 provides the most efficient operating and storage condition ranges required for this board.

Table 2-9. Environmental Requirements

	Processor	300MHz Conditions	533MHz Conditions	1GHz Conditions
Temperature	Operating	+0° to +70°C (32° to +158°F)	+0° to +70°C (32° to +158°F)	+0° to +70°C (32° to +158°F)
	Extended (Optional)	-40° to +85°C (-40° to +185°F)	-40° to +85°C (-40° to+185°F)	-40° to +85°C (-40° to +185°F)
	Storage	–55° to +85°C (–67° to +185°F)	–55° to +85°C (–67° to +185°F)	–55° to +85°C (–67° to +185°F)
Humidity	Operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing
	Non-operating	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU, Northbridge, Southbridge, and voltage regulators are the sources of heat on the board. The LittleBoard 550 is designed to operate at its maximum CPU speed of 300MHz, 533MHz, or 1GHz. All processors and the northbridge require a heatsink, but no fan is required.

Chapter 3 Hardware

Overview

This chapter discusses the chips and features of the connectors in the following order:

- CPU (U1)
- Memory
- PC/104-Plus (J21A, B, C, D)
- PC/104 (J1A, B, C, D)
- IDE Interfaces (J12, J17)
- CompactFlash Adapter (J23)
- Floppy Interface (J14)
- Serial Interfaces (J11, J13)
- Parallel Interface (J15)
- Utility Interfaces (J16, J18, J24)
  - Keyboard
  - Mouse
  - Battery
  - Reset Switch
  - Speaker
  - USB
  - SMBus
- Ethernet Interfaces (J7, J32)
- Audio Interface (J28)
- Video Interfaces (J3, J31)
- Miscellaneous
  - Time of Day/RTC
  - Temperature Monitoring
  - Oops! Jumper (BIOS recovery)
  - Serial Console
  - Watchdog timer
- Power Interface (J10)

NOTE	Ampro Computers, Inc. only supports the features/options tested and listed in this manual. The main integrated circuits (chips) used in the LittleBoard 550 may provide more features or options than are listed for the LittleBoard 550, but some of these chip features/options are not supported on the board and may not function as specified in the chip documentation.

CPU (U1)

The LittleBoard 550 offers three VIA Technologies Eden processor choices; high performance 1GHz ESP 10000 processor, 533MHz ESP 5000 processor, or the low cost, 300MHz ESP3000 processor.

ESP Processors

The ESP (0.13µ or 0.15µ) processors at 1GHz, 533MHz, or 300MHz use 133MHz, 133MHz, or 66MHz FSB (front side bus) respectively, with 128kB Level 1 cache and 64kB Level 2 cache. The ESP processors require a heatsink, but no fan.

NOTE	A CPU fan connector is provided for your convenience to accommodate any special requirements. See Table 3-28.

Memory

The LittleBoard 550 memory consists of the following elements:

- SDRAM
- Flash memory
- Serial EEPROM (SEEP)

SDRAM Memory (DIMM1)

The LittleBoard 550 supports a single standard 168-pin DIMM slot.

- DIMM slot can support up to 2GB of memory
- Supports PC 133 (133MHz, 7.5ns) and PC 100 (100MHz, 10ns)
- +3.3V SDRAM

NOTE	Ampro recommends using only PC 133 (133MHz), 3.3V, 7.5ns, 168-pin, SDRAM DIMM, but PC 100 (100MHz, 10ns) will function. PC 133 provides the best performance for the Eden processors.

Flash Memory (U17)

There is an 8-bit wide, 512kB flash device used for system BIOS that is connected to the Southbridge, VT82C686B, through an ISA bus transceiver. The BIOS is re-programmable and the supported features are detailed in Chapter 4, *BIOS Setup*.

Serial EEPROM (SEEP)

The 2-wire Serial EEPROM (SEEP) contains 4k-bits and at least 512-bit area is reserved for the user. The SEEP is used to store system parameters for battery-free boot capability when there is no battery present. The SEEP uses the SMBus as its 2-wire interface.

Interrupt Channel Assignments

The channel interrupt assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Keyboard		X														
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
COM3				O	O						O	D				
COM4				O	O						D	O				
Floppy							X									
Parallel						O		D								
RTC									X							
IDE Primary															X	O
IDE Secondary															O	X
Math Coprocessor														X		
PS/2 Mouse													X			
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
Sound Blaster						D		O		O	O					
USB	Automatically Assigned															
VGA	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE	The IRQs for the Ethernet, Video, and Internal Local Bus (ISA) are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. Memory below 000500h is used by the BIOS.

Table 3-2. Memory Map

Base Address	Function
00000000h - 0009FFFFh	Conventional Memory
000A0000h - 000AFFFFh	Graphics Memory
000B0000h - 000B7FFFh	Mono Text Memory
000B8000h - 000BFFFFh	Color Text Memory
000C0000h - 000C7FFFh	Standard Video BIOS
000F0000h - 000FFFFFh	System BIOS Area (Storage and RAM Shadowing)
00100000h - 04000000h	Extended Memory (If onboard VGA is enabled, then the amount of memory assigned is subtracted from extended memory)
FFF80000h - FFFFFFFFh	System Flash

I/O Address Map

Table 3-3 shows the I/O address map.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
000-00F	Primary DMA Controller
020-021	Master interrupt Controller
040-043	Programmable Interrupt Timer (Clock/Timer)
060-06F	Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
092	Fast A20 gate and CPU reset
094	Motherboard enable
102	Video subsystem register
0A0-0BF	Slave Interrupt Controller
0C0-0DF	Slave DMA Controller #2
0F0-0FF	Math Coprocessor
170-177	Secondary IDE Hard Disk Controller
1F0-1F8	Primary IDE Hard Disk Controller
278-27F	Parallel Printer
2E8-2FF	Serial Port 4 (COM4)
2F8-2FF	Serial Port 2 (COM2)
378-37F	Parallel port (Standard and EPP)
3C0-3DF	VGA
3E8-3EF	Serial Port 3 (COM3)
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port 1 (COM1)
778-77A	Parallel Port (ECP Extensions) (Port 378+400)
CF8-CFF	PCI bus Configuration Address and Data

PC/104-Plus Interface (J21)

The PC/104-*Plus* uses a 120-pin (30x4) header interface. This interface header carries all of the appropriate PCI signals operating at clock speeds up to 33MHz. The Northbridge, VT8606, integrates a PCI arbiter that supports up to four devices with three external PCI masters. This interface header accepts stackable modules and is located on the top of the board.

Table 3-4 provides the signals and descriptions for the PC/104-Plus bus pin-outs.

NOTE	To conform to the PC/104-Plus standard, a key has been inserted into a specific pin in the PC/104-Plus connector (A1).

Table 3-4. PC/104-Plus Pin/Signal Descriptions (J21)

Pin #	Signal	Input/ Output	Description
1 (A1)	Key		Key pin (Not connected)
2 (A2)	VI/O		+5 volts ±5% power supply
3 (A3)	AD05	T/S	PCI Address and Data Bus Line 5 – There are 32 signal lines (address and data) and the signals on these lines are multiplexed. A bus transaction consists of an address followed by one or more data cycles.
4 (A4)	C/BE0*	T/S	PCI Bus Command/Byte Enable 0 – This signal line is one of four signal lines. These signal lines are multiplexed, so that during the address cycle, the command is defined and during the data cycle, the byte enable is defined.
5 (A5)	GND		Ground
6 (A6)	AD11	T/S	PCI Address and Data Bus Line 11 – Refer to Pin 3 for more information.
7 (A7)	AD14	T/S	PCI Address and Data Bus Line 14 – Refer to Pin 3 for more information.
8 (A8)	+3.3V		+3.3 volts ±5% power supply
9 (A9)	SERR*	O/D	System Error – This signal is for reporting address parity errors.
10 (A10)	GND		Ground
11 (A11)	STOP*	S/T/S	Stop – This signal indicates the current selected device is requesting the master to stop the current transaction
12 (A12)	+3.3V		+3.3 volts ±5% power supply
13 (A13)	FRAME*	S/T/S	PCI bus Frame access – This signal is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle
14 (A14)	GND		Ground
15 (A15)	AD18	T/S	PCI Address and Data Bus Line 18 – Refer to Pin 3 for more information.
16 (A16)	AD21	T/S	PCI Address and Data Bus Line 21 – Refer to Pin 3 for more information.
17 (A17)	+3.3V		+3.3 volts ±5% power supply

Pin #	Signal	Input/ Output	Description
18 (A18)	IDSEL0	In	Initialization Device Select 0 – This signal line is one of four signal lines. These signals are used as the chip-select signals during configuration
19 (A19)	AD24	T/S	PCI Address and Data Bus Line 24 – Refer to Pin 3 for more information.
20 (A20)	GND		Ground
21 (A21)	AD29	T/S	PCI Address and Data Bus Line 29 – Refer to Pin 3 for more information.
22 (A22)	+5V		+5 volts ±5% power supply
23 (A23)	REQ0*	T/S	Bus Request 0 – This signal line is one of three signal lines. These signals indicate the device desires use of the bus to the arbitrator.
24 (A24)	GND		Ground
25 (A25)	GNT1*	T/S	Grant 1 – This signal line is one of three signal lines. These signal lines indicate access has been granted to the requesting device (PCI Masters).
26 (A26)	+5V		+5 volts ±5% power supply
27 (A27)	CLK2	In	PCI clock 2 – This signal line is one of four signal lines. These clock signals provide the timing outputs for four external PCI devices and the timing for all transactions on the PCI bus
28 (A28)	GND		Ground
29 (A29)	+12V		+12 volts ±5% power supply
30 (A30)	NC		Not connected - Reserved
31 (B1)	NC		Not connected - Reserved
32 (B2)	AD02	T/S	PCI Address and Data Bus Line 2 – Refer to Pin 3 for more information.
33 (B3)	GND		Ground
34 (B4)	AD07	T/S	PCI Address and Data Bus Line 7 – Refer to Pin 3 for more information.
35 (B5)	AD09	T/S	PCI Address and Data Bus Line 9 – Refer to Pin 3 for more information.
36 (B6)	VI/O		+5 volts ±5% power supply
37 (B7)	AD13	T/S	PCI Address and Data Bus Lines 13 – Refer to Pin 3 for more information.
38 (B8)	C/BE1*	T/S	PCI Bus Command/Byte Enable 1 – Refer to Pin 4 for more information.
39 (B9)	GND		Ground
40 (B10)	PERR*		Parity Error – This signal is for reporting data parity errors.
41 (B11)	+3.3V		+3.3 volts ±5% power supply
42 (B12)	TRDY*	S/T/S	Target Ready – This signal indicates the selected device's ability to complete the current cycle of transaction. Both IRDY* and TRDY* must be asserted to terminate a data cycle
43 (B13)	GND		Ground
44 (B14)	AD16	T/S	PCI Address and Data Bus Line 16 – Refer to Pin 3 for more information.

Pin #	Signal	Input/ Output	Description
45 (B15)	+3.3V		+3.3 volts ±5% power supply
46 (B16)	AD20	T/S	PCI Address and Data Bus Lines 20 – Refer to Pin 3 for more information.
47 (B17)	AD23	T/S	PCI Address and Data Bus Line 23 – Refer to Pin 3 for more information.
48 (B18)	GND		Ground
49 (B19)	C/BE3*	T/S	PCI Bus Command/Byte Enable 3 – Refer to Pin 4 for more information.
50 (B20)	AD26	T/S	PCI Address and Data Bus Line 26 – Refer to Pin 3 for more information.
51 (B21)	+5V		+5 volts ±5% power supply
52 (B22)	AD30	T/S	PCI Address and Data Bus Line 30 – Refer to Pin 3 for more information.
53 (B23)	GND		Ground
54 (B24)	REQ2*	T/S	Bus Request – This signal indicates this device desires use of the bus to the arbitrator.
55 (B25)	VI/O		+5 volts ±5% power supply
56 (B26)	CLK0	In	PCI clock 0– Refer to Pin 27 for more information
57 (B27)	+5V		+5 volts ±5% power supply
58 (B28)	INTD*	O/D	Interrupt D – This signal is used to request interrupts only for multi-function devices.
59 (B29)	INTA*	O/D	Interrupt A – This signal is used to request an interrupt.
60 (B30)	NC		Not connected - Reserved
61 (C1)	+5		+5 volts ±5% power supply
62 (C2)	AD01	T/S	PCI Address and Data Bus Line 1 – Refer to Pin 3 for more information.
63 (C3)	AD04	T/S	PCI Address and Data Bus Lines 4 – Refer to Pin 3 for more information.
64 (C4)	GND		Ground
65 (C5)	AD08	T/S	PCI Address and Data Bus Line 8 – Refer to Pin 3 for more information.
66 (C6)	AD10	T/S	PCI Address and Data Bus Line 10 – Refer to Pin 3 for more information.
67 (C7)	GND		Ground
68 (C8)	AD15	T/S	PCI Address and Data Bus Line 15 – Refer to Pin 3 for more information.
69 (C9)	SB0*	NC	Snoop Backoff – Not connected
70 (C10)	+3.3V		+3.3 volts ±5% power supply
71 (C11)	LOCK*	S/T/S	Lock – This signal indicates an operation that may require multiple transactions to complete
72 (C12)	GND		Ground
73 (C13)	IRDY*	S/T/S	Initiator Ready – This signal indicates the master's ability to complete the current data cycle of the transaction

Pin #	Signal	Input/ Output	Description
74 (C14)	+3.3V		+3.3 volts ±5% power supply
75 (C15)	AD17	T/S	PCI Address and Data Bus Line 17 – Refer to Pin 3 for more information.
76 (C16)	GND		Ground
77 (C17)	AD22	T/S	PCI Address and Data Bus Line 22 – Refer to Pin 3 for more information.
78 (C18)	IDSEL1		Initialization Device Select 1 – Refer to Pin 18 for more information
79 (C19)	VI/O	NC	(+5V) Not connected
80 (C20)	AD25	T/S	PCI Address and Data Bus Line 25 – Refer to Pin 3 for more information.
81 (C21)	AD28	T/S	PCI Address and Data Bus Line 28 – Refer to Pin 3 for more information.
82 (C22)	GND		Ground
83 (C23)	REQ1*	T/S	Bus Request 1 – Refer to Pin 23 for more information.
84 (C24)	+5V		+5 volts ±5% power supply
85 (C25)	GNT2*	T/S	Grant 2 – Refer to Pin 25 for more information
86 (C26)	GND		Ground
87 (C27)	CLK3	In	PCI clock 3 – Refer to Pin 27 for more information
88 (C28)	+5V		+5 volts ±5% power supply
89 (C29)	INTB*	O/D	Interrupt B – This signal is used to request interrupts only for multi-function devices.
90 (C30)	PME*		Power Management Event – This signal is used for power management events
91 (D1)	AD00	T/S	PCI Address and Data Bus Line 0 – Refer to Pin 3 for more information.
92 (D2)	+5V		+5 volts ±5% power supply
93 (D3)	AD03	T/S	PCI Address and Data Bus Lines 3 – Refer to Pin 3 for more information.
94 (D4)	AD06	T/S	PCI Address and Data Bus Lines 6 – Refer to Pin 3 for more information.
95 (D5)	GND		Ground
96 (D6)	GND		Ground
97 (D7)	AD12	T/S	PCI Address and Data Bus Line 12 – Refer to Pin 3 for more information.
98 (D8)	+3.3V		+3.3 volts ±5% power supply
99 (D9)	PAR	T/S	PCI bus Parity bit – This signal is the even parity bit on AD[31:0] and C/BE[3:0]*
100 (D10)	NC	NC	Not connected (Snoop Done)
101 (D11)	GND		Ground
102 (D12)	Devsel*	S/T/S	Device Select – This signal is driven by the target device when its address is decoded.

Pin #	Signal	Input/ Output	Description
103 (D13)	+3.3V		+3.3 volts ±5% power supply
104 (D14)	C/BE2*		PCI Bus Command/Byte Enable 2 – Refer to Pin 4 for more information.
105 (D15)	GND		Ground
106 (D16)	AD19	T/S	PCI Address and Data Bus Line 19 – Refer to Pin 3 for more information.
107 (D17)	+3.3V		+3.3 volts ±5% power supply
108 (D18)	IDSEL2		Initialization Device Select 2 – Refer to Pin 18 for more information.
109 (D19)	IDSEL3		Initialization Device Select 3 – Refer to Pin 18 for more information.
110 (D20)	GND		Ground
111 (D21)	AD27	T/S	PCI Address and Data Bus Line 27 – Refer to Pin 3 for more information.
112 (D22)	AD31	T/S	PCI Address and Data Bus Line 31 – Refer to Pin 3 for more information.
113 (D23)	VI/O		+5 volts ±5% power supply
114 (D24)	GNT0*	T/S	Grant 0 – Refer to Pin 25 for more information.
115 (D25)	GND		Ground
116 (D26)	CLK1	In	PCI clock 1 – Refer to Pin 27 for more information
117 (D27)	GND		Ground
118 (D28)	RST*	In	PCI bus reset – This signal is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset
119 (D29)	INTC*	O/D	Interrupt C – This signal is used to request interrupts only for multi-function devices.
120 (D30)	GND		Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

The Input/Output signals in this table refer to the input/output signals listed in the *PCI Local Bus Manual*, Revision 2.2, Chapter 2, paragraph 2.1, Signal definitions. The following terms or acronyms are used in this table:

- In – Input is standard input only signal
- Out – Totem Pole output is a standard active driver
- T/S – Tri-State is a bi-directional input output pin
- S/T/S – Sustained Tri-State is an active low tri-state signal driven by one and only one agent at a time
- O/D – Open Drain allows multiple devices to share as a wire-OR.

PC/104 Interface (J1A,B,C,D)

The PC/104 Bus uses a 104-pin 100 mil header interface. This interface header will carry all of the appropriate PC/104 signals operating at clock speeds up to 8MHz. This interface header accepts stackable modules and is located on the top of the board.

NOTE	To conform to the PC/104 standard, keys have been inserted into specific pins in the PC/104 connector (B10, C19).

Table 3-5. PC/104 Interface Pin/Signal Descriptions (J1A)

Pin #	Signal	Description (J1 Row A)
1 (A1)	IOCHCHK*	I/O Channel Check – This signal may be activated by ISA boards to request that a non-maskable interrupt (NMI) be generated to the system processor. It is driven active to indicate uncorrectable error detection.
2 (A2)	SD7	System Data 7 – This signal (0 to 19) provides a system data bit.
3 (A3)	SD6	System Data 6 – Refer to SD7, pin-A2, for more information.
4 (A4)	SD5	System Data 5 – Refer to SD7, pin-A2, for more information.
5 (A5)	SD4	System Data 4 – Refer to SD7, pin-A2, for more information.
6 (A6)	SD3	System Data 3 – Refer to SD7, pin-A2, for more information.
7 (A7)	SD2	System Data 2 – Refer to SD7, pin-A2, for more information.
8 (A8)	SD1	System Data 1 – Refer to SD7, pin-A2, for more information.
9 (A9)	SD0	System Data 0 – Refer to SD7, pin-A2, for more information.
10 (A10)	IOCHRDY	I/O Channel Ready – This signal allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signal's normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read, or write command. The signal is released high when the device is ready to complete the cycle.
11 (A11)	AEN	Address Enable – This signal is used to degate the system processor and other devices from the bus during DMA transfers. When this signal is active, the system DMA controller has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.
12 (A12)	SA19	System Address 19 – This signal (0 to 19) provides a system address bit.
13 (A13)	SA18	System Address 18 – Refer to SA19, pin-A12, for more information.
14 (A14)	SA17	System Address 17 – Refer to SA19, pin-A12, for more information.
15 (A15)	SA16	System Address 16 – Refer to SA19, pin-A12, for more information.
16 (A16)	SA15	System Address 15 – Refer to SA19, pin-A12, for more information.
17 (A17)	SA14	System Address 14 – Refer to SA19, pin-A12, for more information.
18 (A18)	SA13	System Address 13 – Refer to SA19, pin-A12, for more information.
19 (A19)	SA12	System Address 12– Refer to SA19, pin-A12, for more information.
20 (A20)	SA11	System Address 11 – Refer to SA19, pin-A12, for more information.
21 (A21)	SA10	System Address 10 – Refer to SA19, pin-A12, for more information.
22 (A22)	SA9	System Address 9 – Refer to SA19, pin-A12, for more information.

Pin #	Signal	Description (J1 Row A)
23 (A23)	SA8	System Address 8 – Refer to SA19, pin-A12, for more information.
24 (A24)	SA7	System Address 7 – Refer to SA19, pin-A12, for more information.
25 (A25)	SA6	System Address 6 – Refer to SA19, pin-A12, for more information.
26 (A26)	SA5	System Address 5 – Refer to SA19, pin-A12, for more information.
27 (A27)	SA4	System Address 4 – Refer to SA19, pin-A12, for more information.
28 (A28)	SA3	System Address 3 – Refer to SA19, pin-A12, for more information.
29 (A29)	SA2	System Address 2 – Refer to SA19, pin-A12, for more information.
30 (A30)	SA1	System Address 1 – Refer to SA19, pin-A12, for more information.
31 (A31)	SA0	System Address 0 – Refer to SA19, pin-A12, for more information.
32 (A32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-6. PC/104 Interface Pin/Signal Descriptions (J1B)

Pin #	Signal	Descriptions (J1 Row B)
33 (B1)	GND	Ground
34 (B2)	RESETDRV	Reset Drive – This signal is used to reset or initialize system logic on power up or subsequent system reset.
35 (B3)	+5V	+5 volt power ±10%
36 (B4)	IRQ9	Interrupt request 9 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
37 (B5)	-5V	Not connected (-5 volts)
38 (B6)	DRQ2	DMA Request 2 – Used by I/O resources to request DMA service, or to request ownership of the bus as a bus master device. Must be held high until associated DACK2 line is active.
39 (B7)	-12V	Not connected (-12 volts)
40 (B8)	ENDXFR*	Zero Wait State – This signal is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, this signal is derived from an address decode.
41 (B9)	+12V	+12 Volts
42 (B10)	Key	Key Pin (Not connected)
43 (B11)	SMEMW*	System Memory Write – This signal is used by bus owner to request a memory device to store data currently on the data bus and only active for the lower 1MB. Used for legacy compatibility with 8-bit cards.
44 (B12)	SMEMR*	System Memory Read – This signal is used by bus owner to request a memory device to drive data onto the data bus and only active for lower 1MB. Used for legacy compatibility with 8-bit cards.
45 (B13)	IOW*	I/O Write – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to capture the write data on the data bus.
46 (B14)	IOR*	I/O Read – This strobe signal is driven by the owner of the bus (ISA bus master or DMA controller) and instructs the selected I/O device to drive read data onto the data bus.

Pin #	Signal	Descriptions (J1 Row B)
47 (B15)	DACK3*	DMA Acknowledge 3 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
48 (B16)	DRQ3	DMA Request 3 – Used by I/O resources to request DMA service. Must be held high until associated DACK3 line is active.
49 (B17)	DACK1*	DMA Acknowledge 1 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
50 (B18)	DRQ1	DMA Request 1 – Used by I/O resources to request DMA service. Must be held high until associated DACK1 line is active.
51 (B19)	REFRESH*	Memory Refresh – This signal is driven low to indicate a memory refresh cycle is in progress. Memory is refreshed every 15.6 usec.
52 (B20)	SYSCLK	System Clock – This is a free running clock typically in the 8MHz to 10MHz range, although its exact frequency is not guaranteed.
53 (B21)	IRQ7	Interrupt Request 7 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
54 (B22)	IRQ6	Interrupt Request 6 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
55 (B23)	IRQ5	Interrupt Request 5 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
56 (B24)	IRQ4	Interrupt Request 4 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
57 (B25)	IRQ3	Interrupt Request 3 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
58 (B26)	DACK2*	DMA Acknowledge 2 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
59 (B27)	TC	Terminal Count – This signal is a pulse to indicate a terminal count has been reached on a DMA channel operation.
60 (B28)	BALE	Buffered Address Latch Enable – This signal is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AENx, it indicates a valid processor or DMA address.
61 (B29)	+5V	+5 volt power ±10%
62 (B30)	OSC	Oscillator – This clock signal operates at 14.3MHz. This signal is not synchronous with the system clock (SYSCLK).
63 (B31)	GND	Ground
64 (B32)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-7. PC/104 Interface Pin/Signal Descriptions (J1C)

Pin #	Signal	Descriptions (J1 Row C)
1 (C0)	GND	Ground
2 (C1)	SBHE*	System Byte High Enable – This signal is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).
3 (C2)	LA23	Lactchable Address 23 – This signal must be latched by the resource if the line is required for the entire data cycle.
4 (C3)	LA22	Lactchable Address 22 – Refer to LA23, pin-C2, for more information.
5 (C4)	LA21	Lactchable Address 21 – Refer to LA23, pin-C2, for more information.
6 (C5)	LA20	Lactchable Address 20 – Refer to LA23, pin-C2, for more information.
7 (C6)	LA19	Lactchable Address 19 – Refer to LA23, pin-C2, for more information.
8 (C7)	LA18	Lactchable Address 18 – Refer to LA23, pin-C2, for more information.
9 (C8)	LA17	Lactchable Address 17 – Refer to LA23, pin-C2, for more information.
10 (C9)	MEMR*	Memory Read – This signal instructs a selected memory device to drive data onto the data bus. It is active on all memory read cycles.
11 (C10)	MEMW*	Memory Write – This signal instructs a selected memory device to store data currently on the data bus. It is active on all memory write cycles.
12 (C11)	SD8	System Data 8 – Refer to SD7, pin-A2, for more information.
13 (C12)	SD9	System Data 9 – Refer to SD7, pin-A2, for more information.
14 (C13)	SD10	System Data 10 – Refer to SD7, pin-A2, for more information.
15 (C14)	SD11	System Data 11 – Refer to SD7, pin-A2, for more information.
16 (C15)	SD12	System Data 12 – Refer to SD7, pin-A2, for more information.
17 (C16)	SD13	System Data 13 – Refer to SD7, pin-A2, for more information.
18 (C17)	SD14	System Data 14 – Refer to SD7, pin-A2, for more information.
19 (C18)	SD15	System Data 15 – Refer to SD7, pin-A2, for more information.
20 (C19)	Key	Key Pin (Not connected)

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-8. PC/104 Interface Pin/Signal Descriptions (J1D)

Pin #	Signal	Descriptions (J1 Row D)
21 (D0)	GND	Ground
22 (D1)	MEMCS16*	Memory Chip Select 16 – This is signal is driven low by a memory slave device to indicates it is cable of performing a 16-bit memory data transfer. This signal is driven from a decode of the LA23 to LA17 address lines.
23 (D2)	IOCS16*	I/O Chip Select 16 – This signal is driven low by an I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.
24 (D3)	IRQ10	Interrupt Request 10 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
25 (D4)	IRQ11	Interrupt Request 11 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
26 (D5)	IRQ12	Interrupt Request 12 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.

Pin #	Signal	Descriptions (J1 Row D)
27 (D6)	IRQ15	Interrupt Request 15 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
28 (D7)	IRQ14	Interrupt Request 14 – Asserted by a device when it has pending interrupt request. Only one device may use the request line at a time.
29 (D8)	DACK0*	DMA Acknowledge 0 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
30 (D9)	DRQ0	DMA Request 0 – Used by I/O resources to request DMA service. Must be held high until associated DACK0 line is active.
31 (D10)	DACK5*	DMA Acknowledge 5 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
32 (D11)	DRQ5	DMA Request 5 – Used by I/O resources to request DMA service. Must be held high until associated DACK5 line is active.
33 (D12)	DACK6*	DMA Acknowledge 6 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
34 (D13)	DRQ6	DMA Request 6 – Used by I/O resources to request DMA service. Must be held high until associated DACK6 line is active.
35 (D14)	DACK7*	DMA Acknowledge 7 – Used by DMA controller to select the I/O resource requesting the bus, or to request ownership of the bus as a bus master device. Can also be used by the ISA bus master to gain control of the bus from the DMA controller.
36 (D15)	DRQ7	DMA Request 7 – Used by I/O resources to request DMA service. Must be held high until associated DACK7 line is active.
37 (D16)	+5V	+5 volt power ±10%
38 (D17)	MASTER*	Bus Master Assert – This signal is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.
39 (D18)	GND	Ground
40 (D19)	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

IDE Interface (J12, J17)

The LittleBoard 550 provides two IDE connectors for primary and secondary IDE signals.

The EIDE interface logic supports the following features:

- Transfer rate up to 100Mbps
- Increase reliability using Ultra DMA 33/66/100 transfer protocols
- Full scatter-gather capability
- Supports ATAPI and DVD compliant devices
- PIO IDE transfers as fast as 14Mbps.
- Bus master IDE transfers as fast as 100Mbps.
- Single Bus Master EIDE
- Supports two IDE drives per interface channel (primary or secondary connector)

Table 3-9 gives the signals for the IDE 40-pin, 0.100" header.

Table 3-9. Primary IDE Interface Pin/Signal Descriptions (J12)

Pin #	Signal	Description
1	IDERST*	IDE Reset – Low active hardware reset (RSTDRV inverted)
2	GND	Ground
3	PDD7	Primary Disk Data 7 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals.
4	PDD8	Primary Disk Data 8 – Refer to PDD7 on pin-2 for more information.
5	PDD6	Primary Disk Data 6 – Refer to PDD7on pin-2 for more information.
6	PDD9	Primary Disk Data 9 – Refer to PDD7on pin-2 for more information.
7	PDD5	Primary Disk Data 5 – Refer to PDD7on pin-2 for more information.
8	PDD10	Primary Disk Data 10 – Refer to PDD7 on pin-2 for more information.
9	PDD4	Primary Disk Data 4 – Refer to PDD7 on pin-2 for more information.
10	PDD11	Primary Disk Data 11 – Refer to PDD7 on pin-2 for more information.
11	PDD3	Primary Disk Data 3 – Refer to PDD7 on pin-2 for more information.
12	PDD12	Primary Disk Data 12 – Refer to PDD7 on pin-2 for more information.
13	PDD2	Primary Disk Data 2 – Refer to PDD7 on pin-2 for more information.
14	PDD13	Primary Disk Data 13 – Refer to PDD7 on pin-2 for more information.
15	PDD1	Primary Disk Data 1 – Refer to PDD7 on pin-2 for more information.
16	PDD14	Primary Disk Data 14 – Refer to PDD7 on pin-2 for more information.
17	PDD0	Primary Disk Data 0 – Refer to PDD7 on pin-2 for more information.
18	PDD15	Primary Disk Data 15 – Refer to PDD7 on pin-2 for more information.
19	GND	Ground
20	NC/Key	Not connected / Key pin plug

Pin #	Signal	Description
21	PDREQ	Primary DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by PDIOR* and PDIOW*). Also used in an asynchronous mode with PDACK*. Drive asserts PDREQ when ready to transfer or receive data.
22	GND	Ground
23	PDIOW*	Primary I/O Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Ground
25	PDIOR*	Primary I/O Read Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Ground
27	PDIORDY	Primary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	NU	Not used (Pull down to ground through 470 ohm resistor)
29	PDACK*	Primary DMA Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to PDREQ asserted.
30	GND	Ground
31	IRQ14	Interrupt Request 14 – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
32	NC	Not connected
33	PDA1	Primary Disk Address 1 – One of three signals (0 – 2) used to indicate which byte in the ATA command block or control block is being accessed.
34	PD33_66	UDMA 33/66 Sense – Used to detect the presence of an 80 conductor IDE cable on the primary IDE channel. Enables BIOS to sense which DMA mode to use for IDE devices.
35	PDA0	Primary Disk Address 0 – Refer to PDA1 on pin-33 for more information.
36	PDA2	Primary Disk Address 2 – Refer to PDA1 on pin-33 for more information.
37	PDCS1#	Primary Slave/Master Chip Select 1 – Used to select the host-accessible Command Block Register.
38	PDCS3#	Primary Slave/Master Chip Select 3 – Used to select the host-accessible Command Block Register.
39	IDEPACT	Connected through 10k ohm resistor to +5V
40	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Table 3-10. Secondary IDE Interface Pin/Signal Descriptions (J17)

Pin #	Signal	Description
1	IDERST*	IDE Reset – Low active hardware reset (RSTDRV inverted)
2	GND	Ground
3	SDD7	Secondary Disk Data 7 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word.

Pin #	Signal	Description
		All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals.
4	SDD8	Secondary Disk Data 8 – Refer to SDD7 on pin-2 for more information.
5	SDD6	Secondary Disk Data 6 – Refer to SDD7 on pin-2 for more information.
6	SDD9	Secondary Disk Data 9 – Refer to SDD7 on pin-2 for more information.
7	SDD5	Secondary Disk Data 5 – Refer to SDD7 on pin-2 for more information.
8	SDD10	Secondary Disk Data 10 – Refer to SDD7 on pin-2 for more information.
9	SDD4	Secondary Disk Data 4 – Refer to SDD7 on pin-2 for more information.
10	SDD11	Secondary Disk Data 11 – Refer to SDD7 on pin-2 for more information.
11	SDD3	Secondary Disk Data 3 – Refer to SDD7 on pin-2 for more information.
12	SDD12	Secondary Disk Data 12 – Refer to SDD7 on pin-2 for more information.
13	SDD2	Secondary Disk Data 2 – Refer to SDD7 on pin-2 for more information.
14	SDD13	Secondary Disk Data 13 – Refer to SDD7 on pin-2 for more information.
15	SDD1	Secondary Disk Data 1 – Refer to SDD7 on pin-2 for more information.
16	SDD14	Secondary Disk Data 14 – Refer to SDD7 on pin-2 for more information.
17	SDD0	Secondary Disk Data 0 – Refer to SDD7 on pin-2 for more information.
18	SDD15	Secondary Disk Data 15 – Refer to SDD7 on pin-2 for more information.
19	GND	Ground
20	NC/Key	Not connected / Key pin plug
21	SDREQ	Secondary DMA Request – Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Also used in an asynchronous mode with SDACK*. Drive asserts SDREQ when ready to transfer or receive data.
22	GND	Ground
23	SDIOW*	Secondary I/O Write Strobe – Strobe signal for write functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
24	GND	Ground
25	SDIOR*	Secondary I/O Read Strobe – Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.
26	GND	Ground
27	SDIORDY	Secondary I/O Channel Ready – When negated extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
28	NU	Not used (Pull down to ground through 470 ohm resistor)
29	SDDACK*	Secondary DMA Acknowledge – Used by the host to acknowledge data has been accepted or data is available. Used in response to DMARQ asserted.
30	GND	Ground
31	IRQ15	Interrupt Request 15 – Asserted by drive when it has pending interrupt (PIO transfer of data to or from the drive to the host).
32	NC	Not connected

Pin #	Signal	Description
33	SDA1	Secondary Disk Address 1 – One of three signals (0 – 2) used to indicate which byte in the ATA command block or control block is being accessed.
34	SD33_66	UDMA 33/66 Sense – Used to detect the presence of an 80 conductor IDE cable on the secondary IDE channel. Enables BIOS to sense which DMA mode to use for IDE devices.
35	SDA0	Secondary Disk Address 0 – Refer to SDA1 on pin-33 for more information.
36	SDA2	Secondary Disk Address 2 – Refer to SDA1 on pin-33 for more information.
37	SDCS1#	Secondary Slave/Master Chip Select 1 – Used to select the host-accessible Command Block Register.
38	SDCS3#	Secondary Slave/Master Chip Select 3 – Used to select the host-accessible Command Block Register.
39	Reserved	Reserved
40	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

CompactFlash Adapter (J23)

The board contains a Type II PC card socket, which allows for the insertion of a CompactFlash Card. The CompactFlash (CF) Card acts as a standard IDE Drive and is connected to the primary IDE bus. If a CompactFlash card is installed, only one additional IDE drive may be added to the primary bus. Jumpers are used to select the Master/Slave mode and the voltage selection (+5V or +3.3V). Refer to Table 2-4, Jumper Settings for more information.

Table 3-11. CompactFlash Interface Pin/Signal Descriptions (J23)

Pin #	Signal	Description
1	GND	Ground
2	PDD3	Disk Data 3 – These signals (D0-D15) carry the Data, Commands, and Status between the host and the controller. D0 is the LSB of the even Byte of the Word. D8 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D0-D7, while all data transfers are 16 bit using D0-D15 to provide the disk data signals.
3	PDD4	Disk Data 4 – Refer to PDD3 on pin-2 for more information.
4	PDD5	Disk Data 5 – Refer to PDD3 on pin-2 for more information.
5	PDD6	Disk Data 6 – Refer to PDD3 on pin-2 for more information.
6	PDD7	Disk Data 7 – Refer to PDD3 on pin-2 for more information.
7	PDCE1*	Primary Chip Select 1 – This signal, along with CE2*, selects the card and indicates when a byte or word operation is being performed. This signal accesses the even byte or odd byte of the word depending on A0 and CE2*.
8, 9, 10, 11, 12	GND	Ground
13	VCC	CF power – This voltage is determined by setting of JP3, CF Voltage Select (pins 1-2 = +5 volts ±5% **Default**, or pins 2-3 = +3.3 volts ±5%)
14, 15, 16, 17	GND	Ground
18	PDA2	Primary Disk Address 2 – One of three signals (0 – 2) used to select one of eight registers in the Task File. The host grounds all remaining address lines.
19	PDA1	Primary Disk Address 1 – Refer to A2 on pin-18 for more information.
20	PDA0	Primary Disk Address 0 – Refer to A2 on pin-18 for more information.
21	PDD0	Primary Disk Data 0 – Refer to PDD3 on pin-2 for more information.
22	PDD1	Primary Disk Data 1 – Refer to PDD3 on pin-2 for more information.
23	PDD2	Primary Disk Data 2 – Refer to PDD3 on pin-2 for more information.
24	NC	Not connected (IOCS16*)
25	GND	Ground
26	NC	Not connected
27	PDD11	Disk Data 11 – Refer to PDD3 on pin-2 for more information.
28	PDD12	Disk Data 12 – Refer to PDD3 on pin-2 for more information.
29	PDD13	Disk Data 13 – Refer to PDD3 on pin-2 for more information.
30	PDD14	Disk Data 14 – Refer to PDD3 on pin-2 for more information.

Pin #	Signal	Description
31	PDD15	Disk Data 15 – Refer to PDD3 on pin-2 for more information.
32	PDCE2*	Primary Slave/Master Chip Select – This signal, along with CE1*, selects the CompactFlash card and indicates to the card when a byte or word operation is being performed. This signal always accesses the odd byte of the word.
33	NC	Not Connected (VS1*)
34	PDIOR*	Primary I/O Read Strobe – This signal is generated by the host and gates the I/O data onto the bus from the CompactFlash card when the card is configured to use the I/O interface.
35	PDIOW*	Primary I/O Write Strobe – This signal is generated by the host and clocks the I/O data on the Card Data bus into the CompactFlash card controller registers when the card is configured to use the I/O interface. The clock occurs on the negative to positive edge of the signal (trailing edge).
36, 38	VCC	CF power – This voltage is determined by setting of JP3, CF Voltage Select (pins 1-2 = +5 volts ±5% **Default,** or pins 2-3 = +3.3 volts ±5%)
37	IRQ14	Interrupt Request 14 – IRQ 14 is asserted by drive (CF) when it has a pending interrupt (PIO transfer of data to or from the drive to the host).
39	Master*	Master/Slave – This pin determines the Master or Slave configuration of the CompactFlash by the jumper (JP4) setting. When this pin is grounded (jumper inserted), this device is configured as Master. When this pin is open (jumper removed), this device is configured as Slave.
40	NC	Not Connected (VS2*)
41	PDRST*	Primary IDE Reset – This input signal is the active low hardware reset from the host. If this pin goes high, it is used as the reset signal. This pin is driven high at power-up, causing a reset, and if left high will cause another reset.
42	PDIORDY	Primary I/O-DMA Channel Ready – When negated, extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.
43	NC	Not Connected (INPACK)
44	VCC	CF power – This voltage is determined by setting of JP3, CF Voltage Select (pins 1-2 = +5 volts ±5% **Default**, or pins 2-3 = +3.3 volts ±5%)
45	NU	Not used (Pull-up to VCC through 10k ohm resistor)
46	PD33/66	UDMA 33/66 Sense – Senses which DMA mode to use for the CF card.
47	D8	Disk Data – These signals (0 to 15) provide the disk data signals
48	D9	Disk Data – These signals (0 to 15) provide the disk data signals
49	D10	Disk Data – These signals (0 to 15) provide the disk data signals
50	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

CAUTION	To prevent system hangs when using older CompactFlash cards, ensure your CompactFlash is compatible with UDMA 100 IDE hard disk drives. Consult your CompactFlash card vendor for UDMA 100 compatibility.

Floppy Drive Interface (J14)

The VT82C686B chip provides the floppy controller and supports two floppy drives. The floppy signals are provided through the standard 34-pin connector (J14).

The floppy controller will support the 360k, 720k, 1.2M, 1.44M, and 2.88M drives. USB floppy disk drives are also supported.

Table 3-12. Floppy Drive Interface Pin/Signal Descriptions (J14)

Pin #	Signal	Description
2	DRVEN0	Drive (Floppy) Density Select 0
4	NC	Not connected
6	NC	Not connected (DRATE0)
8	INDEX	Index – Sense to detect that the head is positioned over the beginning of a track
10	MTR0	Motor Control 0 – Select drive motor 0.
12	DS1	Drive Select 1 – Select drive 1.
14	DS0	Drive Select 0 – Select drive 0.
16	MTR1	Motor Control 1 – Select drive motor 1.
18	DIR	Direction – Direction of head movement (0 = inward motion, 1 = outward motion).
20	STEP	Step – Low pulse for each track-to-track movement of the head.
22	WDATA	Write Data – Encoded data to the drive for write operations.
24	WGATE	Write Gate – Signal to the drive to enable current flow in the write head.
26	TRK0	Track 0 – Sense detects the head is positioned over track 0.
28	WRTPRT	Write Protect – Senses the diskette is write protected.
30	RDATA	Read Data – Raw serial bit stream from the drive for read operations.
32	HDSEL	Head Select – Selects the side for Read/Write operations (0 = side 1, 1 = side 0)
34	DSKCHG	Disk Change – Senses the drive door is open or the diskette has been changed since the last drive selection.
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33	GND	Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Parallel Port Interface (J15)

Parallel port supports standard parallel, Bi-directional, ECP and EPP protocols. The VIA Southbridge provides the parallel port interface signals.

Table 3-13. Parallel Interface Pin/Signal Descriptions (J15)

Pin #	Signal	In/Out	Description
1	Strobe*	Out	Strobe* – This is an output signal used to strobe data into the printer. I/O pin in ECP/EPP mode.
2	AUTOFDX*	Out	Auto Feed * – This is a request signal into the printer to automatically feed one line after each line is printed.
3	PD0	I/O	Parallel Port Data 0 – This pin (0 to 7) provides parallel port data signals.
4	ERR*	Out	Error – This printer output status indicates an error condition on the printer if the signal state is Low.
5	PD1	I/O	Parallel Port Data 1 – Refer to pin 3 for more information.
6	INIT*	Out	Initialize * – This signal is used to Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
7	PD2	I/O	Parallel Port Data 2 – Refer to pin 3 for more information.
8	SLCTIN	Out	Select In – This output signal is used to select the printer. I/O pin in ECP/EPP mode.
9	PD3	I/O	Parallel Port Data 3 – Refer to pin 3 for more information.
10	GND		Ground
11	PD4	I/O	Parallel Port Data 4 – Refer to pin 3 for more information.
12	GND		Ground
13	PD5	I/O	Parallel Port Data 5 – Refer to pin 3 for more information.
14	GND		Ground
15	PD6	I/O	Parallel Port Data 6 – Refer to pin 3 for more information.
16	GND		Ground
17	PD7	I/O	Parallel Port Data 7 – Refer to pin 3 for more information.
18	GND		Ground
19	ACK*	In	Acknowledge * – This printer output status indicates it has received the data and is ready to accept new data if the signal state is Low.
20	GND		Ground
21	BUSY	In	Busy – This printer output status indicates the printer is not ready to accept data if the signal state is High.
22	GND		Ground
23	PE	In	Paper End – This printer output status indicates the printer is out of paper if the signal state is High.
24	GND		Ground
25	SLCT	In	Select – This printer output status indicates the printer is selected and powered on if the signal state is High.
26	GND		Ground

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Serial Interfaces (J11, J13)

Two chips provide the circuitry for the 4 serial ports. The VT86C686B provides serial ports 1 and 2 through connector J11 and the Super I/O provides serial ports 3 and 4 through connector J13. The four serial ports support the following features:

- Four individual 16550-compatible UARTs
- Programmable word length, stop bits and parity
- 16-bit programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial A Interface (J11)
  - Serial Port 1 (COM1) supports RS232/RS485/RS422 and full modem support
  - Serial Port 2 (COM2) supports RS232/RS485/RS422
- Serial B Interface (J13)
  - Serial Port 3 (COM3) supports RS232/RS485/RS422 and full modem support
  - Serial Port 4 (COM4) supports RS232/RS485/RS422

NOTE	The RS232 and RS485/RS422 modes can be selected for any serial port in BIOS Setup under BIOS and Hardware Settings menu screen. However, the RS232 mode is the default selection (Standard) for any serial port. Refer to the topic **On-Board Serial Ports** under *Power Management and Advanced User Options* in Chapter 4, *BIOS Setup* for more information.

To implement the two-wire RS485 mode on any serial port, you must tie the equivalent pins together for each port.

For example; on Serial Port 1, tie pin 3 to 5 and pin 4 to 6 at the Serial A interface connector (J11) as shown in Figure 3-1. As an alternate, tie pin 2 to 3 and pin 7 to 8 at the DB9 serial connector for Serial Port 1 as shown in Figure 3-1. Refer also to the following tables for the specific pins for the other ports on each connector. The RS422 mode uses a four-wire interface and does not need any pins tied together, but you must select RS485 in BIOS Setup.

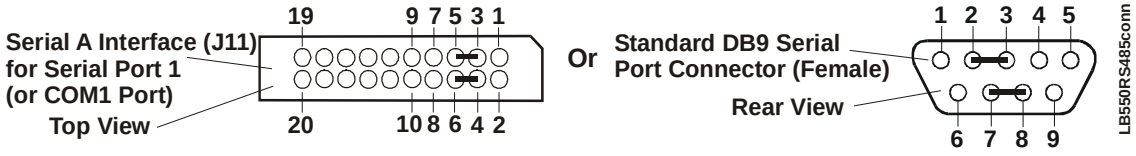


Figure 3-1. RS485 Serial Port Implementation

Table 3-14 gives the pins and corresponding signals for the Serial A interface connector (Serial Ports 1 and 2) and Table 3-15 gives the pins and corresponding signals for the Serial B interface connector (Serial Ports 3 and 4).

Table 3-14. Serial A Interface Pin/Signal Descriptions (J11)

Pin #	Pin # DB9	Signal	Description
1	1 (COM1)	DCD1*	Data Carrier Detect 1 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR1 as part of the DTR/DSR handshake.
2	6	DSR1*	Data Set Ready 1 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR1 for overall readiness to communicate.
3	2	RXD1 RX1-	Receive Data 1 – Serial port 1 receive data in. RX1- – If in RS485 or RS422 mode, this pin is Receive Data 1 -.
4	7	RTS1* TX1+	Request To Send 1 – Indicates Serial port 1 is ready to transmit data. Used as hardware handshake with CTS1 for low level flow control.. TX1+ – If in RS485 or RS422 mode, this pin is Transmit Data 1 +.
5	3	TXD1 TX1-	Transmit Data 1 – Serial port 1 transmit data out. TX1- – If in RS485 or RS422 mode, this pin is Transmit Data 1 -.
6	8	CTS1* RX1+	Clear To Send 1 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS1 for low level flow control. RX1+ – If in RS485 or RS422 mode, this pin is Receive Data 1 -.
7	4	DTR1*	Data Terminal Ready 1 – Indicates Serial port 1 is powered, initialized, and ready. Used as hardware handshake with DSR1 for overall readiness to communicate.
8	9	RI1*	Ring Indicator 1 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND	Ground
10	NC	KEY/ NC	Key Not connected
11	1 (COM2)	DCD2*	Data Carrier Detect 2 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR2 as part of the DTR/DSR handshake.
12	6	DSR2*	Data Set Ready 2 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR2 for overall readiness to communicate.
13	2	RXD2 RX2-	Receive Data 2 – Serial port 2 receive data in RX1- – If in RS485 or RS422 mode, this pin is Receive Data 2 -.
14	7	RTS2* TX2+	Request To Send 2 – Indicates Serial port 2 is ready to transmit data. Used as hardware handshake with CTS2 for low level flow control. TX2+ – If in RS485 or RS422 mode, this pin is Transmit Data 2 +.
15	3	TXD2 TX2-	Transmit Data 2 – Serial port 2 transmit data out TX2- – If in RS485 or RS422 mode, this pin is Transmit Data 2 -.

Pin #	Pin # DB9	Signal	Description
16	8	CTS2*	Clear To Send 2 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS2 for low level flow control.
		RX2+	RX2+ – If in RS485 or RS422 mode, this pin is Receive Data 2 -.
17	4	DTR2*	Data Terminal Ready 2 – Indicates Serial port 2 is powered, initialized, and ready. Used as hardware handshake with DSR2 for overall readiness to communicate.
18	9	NC	Not Connected (Ring Indicator 2)
19	5	GND	Ground
20	NC	NC	Not connected

Notes: The shaded area denotes power or ground. Signals are listed in the following order RS232 and RS485/RS422.

Table 3-15. Serial B Interface Pin/Signal Descriptions (J13)

Pin #	Pin # DB9	Signal	Description
1	1 (COM3)	DCD3*	Data Carrier Detect 3 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR3 as part of the DTR/DSR handshake.
2	6	DSR3*	Data Set Ready 3 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR3 for overall readiness to communicate.
3	2	RXD3	Receive Data 3 – Serial port 3 receive data in
		RX3-	RX3- – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
4	7	RTS3*	Request To Send 3 – Indicates Serial port 3 is ready to transmit data. Used as hardware handshake with CTS3 for low level flow control.
		TX3+	TX3+ – If in RS485 or RS422 mode, this pin is Transmit Data 3 +.
5	3	TXD3	Transmit Data 3 – Serial port 3 transmit data out
		TX3-	TX3- – If in RS485 or RS422 mode, this pin is Transmit Data 3 -.
6	8	CTS3*	Clear To Send 3 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS3 for low level flow control.
		RX3+	RX3+ – If in RS485 or RS422 mode, this pin is Receive Data 3 -.
7	4	DTR3*	Data Terminal Ready 3 – Indicates Serial port 3 is powered, initialized, and ready. Used as hardware handshake with DSR3 for overall readiness to communicate.
8	9	RI3*	Ring Indicator 3 – Indicates external serial communications device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	5	GND	Ground
10	NC	KEY/	Key
		NC	Not connected

Pin #	Pin # DB9	Signal	Description
11	1 (COM4)	DCD4*	Data Carrier Detect 4 – Indicates external serial communications device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input will be driven by DTR4 as part of the DTR/DSR handshake.
12	6	DSR4*	Data Set Ready 4 – Indicates external serial communications device is powered, initialized, and ready. Used as hardware handshake with DTR4 for overall readiness to communicate.
13	2	RXD4 RX4-	Receive Data 4 – Serial port 4 receive data in RX4- – If in RS485 or RS422 mode, this pin is Receive Data 4 -.
14	7	RTS4* TX4+	Request To Send 4 – Indicates Serial port 4 is ready to transmit data. Used as hardware handshake with CTS4 for low level flow control. TX4+ – If in RS485 or RS422 mode, this pin is Transmit Data 4 +.
15	3	TXD4 TX4-	Transmit Data 4 – Serial port 4 transmit data out TX4- – If in RS485 or RS422 mode, this pin is Transmit Data 4 -.
16	8	CTS4* RX4+	Clear To Send 4 – Indicates external serial communications device is ready to receive data. Used as hardware handshake with RTS4 for low level flow control. RX4+ – If in RS485 or RS422 mode, this pin is Receive Data 4 +.
17	4	DTR4*	Data Terminal Ready 4 – Indicates Serial port 4 is powered, initialized, and ready. Used as hardware handshake with DSR4 for overall readiness to communicate.
18	9	NC	Not connected (Ring Indicator 4)
19	5	GND	Ground
20	NC	NC	Not connected

Notes: The shaded area denotes power or ground. Signals are listed in the following order: RS232 followed by RS485/RS422

Utility Interfaces

The Utility interfaces consists of three connectors that provide the standard interface signals, which include the:

- Utility 1
  - Keyboard
  - External battery connection
  - Reset Switch
  - PC Speaker
- Utility 2
  - PS/2 Mouse
  - SMBus signals
  - USB signals for USB ports 1 and 2
  - Power button signal
- Utility 3
  - USB signals for USB ports 3 (USB0) and 4 (and USB1)

Utility 1 Interface (J16)

Utility 1 interface consists of a 16-pin connector and is used to interface the various utility signals to an external board with external connections or directly to the respective connector, such as, a keyboard, speaker, etc. Table 3-17 gives the pin outs and interface signals for the Utility 1 interface.

- Keyboard
- Battery
- Reset Switch
- Speaker

Keyboard Interface

The signal lines for the PS/2 keyboard are provided through the Utility 1 interface (J16), which is also fully PC/AT compatible.

External Battery

An external battery input connection is provided through the Utility 1 interface (J16) for the Real Time Clock's operation in the event the on-board battery is not used.

Reset Switch

The signal lines for a reset switch (hard or soft) are provided through the Utility 1 interface (J16).

NOTE	To perform the equivalent of a power-on reset, the reset button must be pressed and held for a minimum of three seconds.

PC Speaker

The signal lines for a speaker port with 0.1-watt drive are provided through a Utility 1 interface (J16).

Table 3-16. Utility 1 Interface Pin/Signal Descriptions (J16)

Pin #	Signal	I/O	Description
1	-12	I	-12 volts external supplied through I/O Interface board
2	GND	I	Ground
3	-5V	I	-5 volts external supplied through I/O Interface board
4	GND	I	Ground
5	NU	O	Not used (Power On LED)
6	NC	-	Not connected (PWR Good)
7	SPKR+	O	Speaker + Output
8	GND	I	Ground
9	RSTSW	I	Reset Switch
10	NC	-	Not connected (KBD SW)
11	KBDATA	I/O	Keyboard Data
12	KBCLK	I/O	Keyboard Clock
13	GND	I	Keyboard Ground
14	KBD PWR	O	+5V for Keyboard
15	BATV+	I	+Backup Battery Voltage
16	BATV-	I	Ground (Battery voltage return)

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Utility 2 Interface (J24)

The Utility 2 interface consists of a 24-pin connector used to interface various signals to the external board with external connections, or directly to the respective connector such as, the mouse, etc. Table 3-19 gives the pin outs and interface signals for Utility 2 interface (J24).

- PS/2 Mouse signals
- SMBus signals
- USB signals for USB ports 1 and 2
- Power button signal

Mouse Interface

The signal lines for a PS/2 mouse are provided through the Utility 2 interface (J24).

System Management Bus (SMBus)

The Southbridge chip, VT82C686B, contains both a host and slave SMBus port; but the host cannot access the slave internally. The slave port allows an external master access to the Southbridge through the connector (J24). The master contained in the VT82C686B is used to communicate with the SEEP, SDRAM EPROM, MAX1617, and the clock generator. Table 3-17 gives the addresses for these devices with the components and corresponding binary addresses of the SMBus.

Table 3-17. SMBus Reserved Addresses

Component	Address Binary
Serial EEPROM (SEEP)	$1010,010x_b$
SDRAM EPROM	$1010,000x_b$
Clock Generator (ICS9250)	$1101,001x_b$
Southbridge (VT82C686B)	$0000,000x_b$ (default) Programmable Master
Thermal Sensor (MAX1617)	$0011,0010x_b$

USB Signals (USB0 and USB1)

The LittleBoard 550 contains one root USB hub with four functional USB ports. This connector (Utility 2) provides two of the four USB ports (USB0 and USB1). The hub is USB v.1.1 and Intel Universal HCI v.1.1 compatible.

Features implemented in the USB ports include the following:

- One root hub and two USB ports on this connector
- USB v.1.1 and Intel Universal HCI v.1.1 compatible
- Integrated physical layer transceivers
- Over-current detection status (software) on all four USB ports
- Over-current fuses for all four ports on the LittleBoard 550 board. See Table 2-3.

NOTE	Ampro does not recommend connecting a USB boot device to the LittleBoard 550 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 550. Refer to Chapter 4, BIOS Setup for more information.

Table 3-18. Utility 2 Interface Pin/Signal Descriptions (J24)

Pin #	Signal	I/O	Description
1	SUSC*	-	Lid Switch
2	PWRBT*	I	Power Button
3	BATLOW*	I-	Low Battery
4	NC	O	Not Connected (IR Mode Select)
5	Reserved	O	Reserved (IrDA Transmit)
6	Reserved	I	Reserved (IrDA Receive)
7	GND	-	Ground
8	VCC	-	+5 volts
9	MDATA	I/O	Mouse Data
10	MCLK	I/O	Mouse Clock
11	GND	-	Ground
12	VCC	-	+5 volts
13	SMBCLK	-	SMBus Clock
14	SMBDATA	-	SMBus Data
15	USB1PWR	-	+5V USB 1 Port Power – Port is disabled if this input is low.
16	USB2PWR	-	+5V USB 2 Port Power – Port is disabled if this input is low.
17	USBP1-	I/O	Universal Serial Bus Port 1 Data Negative
18	USBP2-	I/O	Universal Serial Bus Port 2 Data Negative
19	USBP1+	I/O	Universal Serial Bus Port 1 Data Positive
20	USBP2+	I/O	Universal Serial Bus Port 2 Data Positive
21	USB1GND	-	USB 1 Port ground
22	USB2GND	-	USB 2 Port ground
23	SHIELD1	-	USB 1 Port shield (Cable Shield)
24	SHIELD2	-	USB 2 Port shield (Cable Shield)

Notes: The shaded area denotes power or ground. The signals marked with * = Negative true logic.

Utility 3 Interface (J18)

The Utility 3 interface is a 10-pin connector used to provide the two of the USB port signals to an external board with USB connections or directly to the respective USB connector for the USB ports. Table 3-19 gives the pin outs and interface signals for Utility 3 interface.

- USB ports 2 (USB2) and 3 (USB3)

USB Signals (USB2 and USB3)

The LittleBoard 550 contains one root USB hub with four functional USB ports. This connector (Utility 3) provides two (USB2 and USB3) of the four USB ports. The hub is USB v.1.1 and Intel Universal HCI v.1.1 compatible.

Features implemented for the USB ports include the following:

- One root hub and two USB ports on this connector
- USB v.1.1 and Intel Universal HCI v.1.1 compatible
- Integrated physical layer transceivers
- Over-current detection status on the USB port (software)
- Over-current fuses for all four ports on the LittleBoard 550 board. See Table 2-3.

NOTE	Ampro does not recommend connecting a USB boot device to the LittleBoard 550 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 550. Refer to Chapter 4, BIOS Setup for more information.

Table 3-19. Utility 3 Interface Pin/Signal Descriptions (J18)

Pin #	Signal	I/O	Description
1	USB3PWR	-	+5V USB 3 Port Power – Port is disabled if this input is low.
2	USB4PWR	-	+5V USB 4 Port Power – Port is disabled if this input is low.
3	USBP3-	I/O	Universal Serial Bus Port 3 Data Negative
4	USBP4-	I/O	Universal Serial Bus Port 4 Data Negative
5	USBP3+	I/O	Universal Serial Bus Port 3 Data Positive
6	USBP4+	I/O	Universal Serial Bus Port 4 Data Positive
7	USB3GND	-	USB 3 Port ground
8	USB4GND	-	USB 4 Port ground
9	SHIELD3	-	USB 3 Port shield (Cable Shield)
10	SHIELD4	-	USB 4 Port shield (Cable Shield)

Notes: The shaded area denotes power or ground.

Ethernet Interfaces (J7, J32)

The Ethernet solution is provided by two Intel 82551ER PCI controller chips, which consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. The 82551ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82551ER to perform high-speed data transfers over the PCI bus. The 82551ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU.

- Backward software compatible to the 82559, 82558, and 82557
- Chained memory structure
- Full duplex or half-duplex support
- Full duplex support at 10Mbps and 100Mbps
- In half-duplex mode, performance is enhanced by a proprietary collision reduction mechanism.
- IEEE 802.3 10BaseT/100BaseT compatible physical layer to wire transformer
- 2 LED support for each port (link/activity are shared and speed)
- Data transmission with minimum interframe spacing (IFS).
- IEEE 802.3u Auto-Negotiation support with IEEE 802.3x 100BASE-TX flow control support
- 3KB transmit and 3KB receive FIFOs (helps prevent data underflow and overflow)
- Improved dynamic transmit chaining with multiple priorities transmit queues
- Each Ethernet port has a RJ-45 connector and the related magnetics integrated on the board.
- Each Ethernet port controller connected to Primary PCI bus

CAUTION	The two Ethernet ports share a common ground, that is floating until you determine how the grounds are connected, to signal ground or chassis ground.

Tables 3-20 and 3-21 describe the pin-outs and signals of two Ethernet ports 1 and 2, respectively.

Table 3-20. Ethernet Port 1 Pin/Signal Descriptions (J7)

Pin #	Signal	Description
1	TX+	Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals interface directly with an isolation transformer.
2	TX-	
3	RX	Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer.
6	RX-	
4, 5	Term	Termination
7, 8	Term	Termination
9	Speed	Speed signals (10BaseT or 100BaseT transfer rate) to the Green LED
10	3.3V	+3.3 volts +/- 5%
11	Link	Link signals for yellow LED
12	Activity	Activity signals for yellow LED
13, 14	Shld	Grounded Shield

Note: Termination involves connecting a 75 ohm resistor between the connector and a capacitance plane created on an inner layer power plane.

Table 3-21. Ethernet Port 2 Pin/Signal Descriptions (J32)

Pin #	Signal	Description
1	TX+	Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair Cable (UTP). These signals interface directly with an isolation transformer.
2	TX-	
3	RX	Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer.
6	RX-	
4, 5	Term	Termination
7, 8	Term	Termination
9	Speed	Speed signals (10BaseT or 100BaseT transfer rate) to green LED
10	3.3V	+3.3 volts +/- 5%
11	Link	Link signals for yellow LED
12	Activity	Activity signals for yellow LED
13, 14	Shld	Grounded Shield

Note: Termination involves connecting a 75 ohm resistor between the connector and a capacitance plane created on an inner layer power plane.

Audio Interface (J28)

The audio solution on the LittleBoard 550 is provided by the VT82C686B and the LM4549 audio CODEC. These two chips use a digital interface to communicate between the two, which is defined by AC97 and is revision 2.1 compliant. The LittleBoard 550 supports its own audio amplifier (LM4853), which drives the audio signals into an external audio load. Output signals for the audio interface are through the 26-pin 2mm connector (J28) to an external board, which has the respective audio connections on it.

Audio CODEC (LM4549) features

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)
- AC'97 Rev 2.1 compliant
- 3D Sound circuitry
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz
- PC-Beep passthrough to Line Out while reset is held active low
- True Line Level Output with volume control independent of Line Out

Audio Amplifier (LM4853) features

- Dual bridge-connected audio power amplifier
- 2.2W into 4Ω load or 1.1W into 8Ω load.
- Dual Bridge speaker amplifiers
- Stereo headphone amplifier
- External Audio Interface

Table 3-22. Audio Interface Pin/Signal Descriptions (J28)

Pin #	Signal	Description
1	VIDEO_L	Video audio signal in left channel
2	VIDEO_GND	Video digital ground (Audio ground)
3	VIDEO_R	Video audio signal in right channel
4	CD_L	CD-ROM signal left channel
5	CD_GND	CD-ROM digital ground (to Audio CODEC)
6	CD_R	CD-ROM signal right channel
7	LINE_IN_L	Line in signal left channel
8	LINE_IN_GND	Line in digital ground (Audio ground)
9	LINE_IN_R	Line in signal right channel
10	MIC1	Microphone in signal 1 or left channel
11	MIC_GND	Microphone digital ground (Audio ground)
12	MIC2	Microphone in signal 2 or right channel
13	MIC_REF	Microphone reference signal
14	NC/KEY	Not connected - Key pin
15	PHONE_IN	Phone signal in
16	PHONE_GND	Phone digital ground (Audio ground)
17	MONO_OUT	Monaural signal out
18	MONO_GND	Monaural digital ground (Audio ground)
19	+AOUT_L	+ Audio Amplifier output signal left channel
20	AGND	Audio Ground (-AOUT_L)
21	+AOUT_R	+ Audio Amplifier output signal right channel
22	AGND	Audio Ground (-AOUT_R)
23	AGND	Audio Ground
24	HP_L	Headphone signal left channel (from Audio Amp)
25	HP_R	Headphone signal right channel (from Audio Amp)
26	NC	Not connected (Headphone In)

Notes: The shaded area denotes power or ground.

Video Interfaces (J3, J4, J5, J31)

The Northbridge (VT8606) chip provides the graphics control and video signals to the traditional glass CRT monitors and the LCD and LVDS flat panel displays. The chip features are listed below:

CRT features:

- Supports a max resolution of 1600 x 1200 with video frame buffer set at 8MB
- Supports a maximum allowable video frame buffer size of 32MB shared memory
- AGP 4X graphics (always enabled)
- Compliant with Rev 2.0 of AGP Interface

Flat Panel features:

- Supports (3.3V, 5V, or 12V) output to both DSTN and TFT flat panels through a 36-bit interface
- Supports TFT panel sizes from VGA (320x480) up to SXGA+ and UXGA+ (1400x1050).
- Supports LCD VGA and SVGA panels with 9-, 12-, 18-bit interface (1 Pixel/Clock)
- Supports UXGA and SXGA active matrix panels with 1x24-bit interface (2 Pixels/Clock)
- Supports 1 or 2 channel LVDS outputs

CRT Interface

Table 3-23. CRT Interface Pin/Signal Descriptions (J5)

Pin #	Signal	Description
1	RED	Red – This is the Red analog output signal to the CRT.
2	GND	Ground
3	GREEN	Green – This is the Green analog output signal to the CRT.
4	GND	Ground
5	BLUE	Blue – This is the Blue analog output signal to the CRT.
6	GND	Ground
7	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync output to the CRT.
8	GND	Ground
9	VSYNC	Vertical Sync – This signal is used for the digital vertical sync output to the CRT.
10	+5V	+5 volts +/- 5% through Fuse (F5 is next to J5 connector on board)

Notes: The shaded area denotes power or ground.

LCD Interface 1

Table 3-24. LCD Interface 1 Pin/Signal Descriptions (J3)

Pin #	Signal	Description
1	GND	Ground
2	+3.3V	+3.3V
3	+12V	+12V
4	GND	Ground
5	FPCLK	Flat panel shift clock
6	GND	Ground
7	FPDE	Flat panel display enable
8	GND	Ground
9	LP	Line Pulse – This signal is the digital monitor equivalent of HSYNC
10	FLM	First Line Marker – This signal is digital monitor equivalent of VSYNC
11	GND	Ground
12	FP0	Flat Panel Data Output 0 – Mapping for this signal changes with the type of flat panel selected in BIOS Setup. ⊗Refer to the notes for this table.
13	FP1	Flat Panel Data Output 1 – Refer to pin 12 for more information.
14	FP2	Flat Panel Data Output 2 – Refer to pin 12 for more information.
15	FP3	Flat Panel Data Output 3 – Refer to pin 12 for more information.
16	FP4	Flat Panel Data Output 4 –Refer to pin 12 for more information.
17	FP5	Flat Panel Data Output 5 – Refer to pin 12 for more information.
18	FP6	Flat Panel Data Output 6 – Refer to pin 12 for more information.
19	FP7	Flat Panel Data Output 7 – Refer to pin 12 for more information.
20	FP8	Flat Panel Data Output 8 – Refer to pin 12 for more information.
21	FP9	Flat Panel Data Output 9 – Refer to pin 12 for more information.
22	FP10	Flat Panel Data Output 10 – Refer to pin 12 for more information.
23	FP11	Flat Panel Data Output 11 – Refer to pin 12 for more information.
24	FP12	Flat Panel Data Output 12 – Refer to pin 12 for more information.
25	FP13	Flat Panel Data Output 13 – Refer to pin 12 for more information.
26	FP14	Flat Panel Data Output 14 – Refer to pin 12 for more information.
27	FP15	Flat Panel Data Output 15 – Refer to pin 12 for more information.
28	FP16	Flat Panel Data Output 16 – Refer to pin 12 for more information.
29	FP17	Flat Panel Data Output 17 – Refer to pin 12 for more information.
30	FP18	Flat Panel Data Output 18 – Refer to pin 12 for more information.
31	FP19	Flat Panel Data Output 19 – Refer to pin 12 for more information.
32, 33	+5V	+5V +/- %5
34	+3.3V	+3.3V +/- %5
35, 36	NC	Not Connected
37	+3.3V	+3.3V +/- %5
38	ENAVEE	Enable VEE

Pin #	Signal	Description
39	ENAVDD	Power sequencing output for LCD driver
40	GND	Ground
41	FP20	Flat Panel Data Output 20 – Refer to pin 12 for more information.
42	FP21	Flat Panel Data Output 21 – Refer to pin 12 for more information.
43	FP22	Flat Panel Data Output 22 – Refer to pin 12 for more information.
44	+3.3V	+3.3V +/- %5
45	FP23	Flat Panel Data Output 23 – Refer to pin 12 for more information.
46, 47	NC	Not Connected
48, 49	GND	Ground
50	+12V	+12V

Notes: The shaded area denotes power or ground. ⊗Refer to the settings in the BIOS Setup Utility described in Chapter 4, later in this manual and the LittleBoard 550 Software Release Notes.

LCD Interface 2

Table 3-25. LCD Interface 2 Pin/Signal Descriptions (J4)

Pin #	Signal	Description
1, 2	GND	Ground
3	FP24	Flat Panel Data Output 24 – The mapping for this signal changes with the type of flat panel selected in BIOS Setup. ⊗Refer to the notes for this table.
4	FP25	Flat Panel Data Output 25 – Refer to pin 3 for more information.
5	FP26	Flat Panel Data Output 26 – Refer to pin 3 for more information.
6	FP27	Flat Panel Data Output 27 – Refer to pin 3 for more information.
7	FP28	Flat Panel Data Output 28 – Refer to pin 3 for more information. .
8	FP29	Flat Panel Data Output 29 – Refer to pin 3 for more information.
9	FP30	Flat Panel Data Output 30 – Refer to pin 3 for more information. .
10	FP31	Flat Panel Data Output 31 – Refer to pin 3 for more information. .
11	FP32	Flat Panel Data Output 32 – Refer to pin 3 for more information.
12	FP33	Flat Panel Data Output 33 – Refer to pin 3 for more information. .
13	FP34	Flat Panel Data Output 34 – Refer to pin 3 for more information.
14	FP35	Flat Panel Data Output 35 – Refer to pin 3 for more information.
15, 16	GND	Ground

Notes: The shaded area denotes power or ground. ⊗Refer to the settings in the BIOS Setup Utility described in Chapter 4, later in this manual and the LittleBoard 550 Software Release Notes.

LVDS Interface

Table 3-26. LVDS Interface Pin/Signal Descriptions (J31)

Pin #	Signal	Description	Line	Channel
1	3.3V_Panel	+3.3V source	NA	NA
2	5V_Panel	+5V source		
3	GND	Ground		
4	GND	Ground		
5	LVDS_Y0M	Data Negative Output	0	Channel 1
6	LVDS_Y0P	Data Positive Output		
7	LVDS_Y1M	Data Negative Output	1	
8	LVDS_Y1P	Data Positive Output		
9	LVDS_Y2M	Data Negative Output	2	
10	LVDS_Y2P	Data Positive Output		
11	LVDS_CLKYM	Clock Negative Output	Clock	
12	LVDS_CLKYP	Clock Positive Output		
13	LVDS_Z0M	Data Negative Output	0	Channel 2
14	LVDS_Z0P	Data Positive Output		
15	LVDS_Z1M	Data Negative Output	1	
16	LVDS_Z1P	Data Positive Output		
17	LVDS_Z2M	Data Negative Output	2	
18	LVDS_Z2P	Data Positive Output		
19	LVDS_CLKZM	Clock Negative Output	Clock	
20	LVDS_CLKZP	Clock Positive Output		

Notes: The shaded area denotes power or ground.

NOTE	Pins 5-12 constitute 1st channel interface of two channels, or a single channel interface. Pins 13-20 constitute 2nd channel interface of two channels.

Miscellaneous

Real Time Clock (RTC)

The LittleBoard 550 contains a Real Time Clock (RTC) and along with the CMOS RAM are backed up with a Lithium Battery. If the battery is not present or has failed the BIOS has a battery-free boot option to complete the boot process.

Temperature Monitoring

The MAX1617 performs the temperature monitoring function and has an inputs from the thermal diode in the VIA Eden CPUs. The SMBus is connected to a dedicated thermal alert pin in the MAX1617 and the other devices on the SMBus, including the Southbridge (VT82C686B).

NOTE	The LittleBoard 550 requires a heatsink for all VIA Eden CPUs and the Twister-T Northbridge, but no fans.

Oops! Jumper (BIOS Recovery)

The Oops! jumper is provided in the event the BIOS settings you've selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in the EEPROM from being loaded, forcing the use of the default settings. Connect the DTR pin to the RI pin on serial port 1 (COM 1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and go into BIOS Setup. Change the desired BIOS settings, or select the default settings, and save changes before rebooting the system.

To convert the Serial A interface to an Oops! jumper, short together the DTR (7) and RI (8) pins on Serial A (J11) header for Serial Port 1. As an alternate, short the equivalent pins, 4 and 9, on the Serial Port 1 DB9 connector as shown in Figure 3-2.

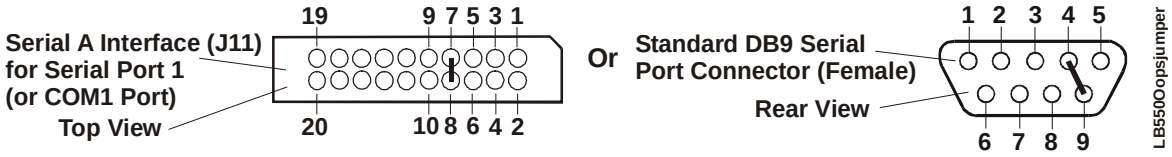


Figure 3-2. Oops! Jumper Connection

Serial Console

The LittleBoard 550 supports the serial console (or console redirection) feature. This I/O function is provided by an ANSI-compatible serial terminal, or the equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by connecting a standard null modem cable or a modified serial cable (or "Hot Cable") between one of the serial ports, such as Serial 1 (J11A), and the serial terminal or a PC with communications software. The BIOS Setup Utility controls the serial console settings on the LittleBoard 550. Refer to Chapter 4, BIOS Setup for the settings of the serial console option, the serial terminal, or PC with communications software and the connection procedure.

Hot (Serial) Cable

To convert a standard serial cable to a Hot Cable, certain pins must be shorted together at the Serial port connector or at the DB9 connector. Short together the RTS (4) and RI (8) pins on Serial A (J11) header,

for the serial port 1. As an alternate, you can short the equivalent pins (pins 7 and 9) on the respective DB9 port connector as shown in Figure 3-3.

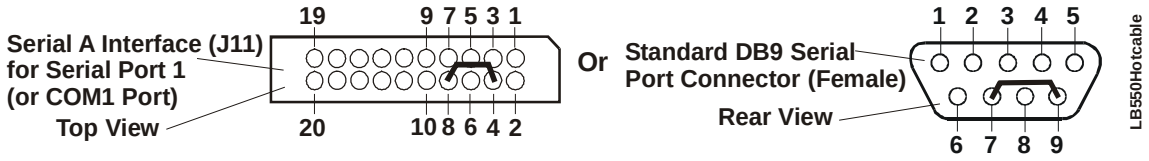


Figure 3-3. Hot Cable Jumper

Watchdog Timer

The watchdog timer (WDT) restarts the system if a mishap occurs, ensuring proper start-up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (watchdog timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT in the Advanced BIOS Features of BIOS Setup. Set the WDT for a time-out interval in seconds, between 2 and 255, in one second increments in the Advanced BIOS Features screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle (turnoff) the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some Ampro Board Support Packages provide an API interface to the WDT. The application must tickle (turnoff) the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

The BIOS implements interrupt 15 function 0C3h to manipulate the WDT.

- Watchdog Code examples – Ampro has provided source code examples on the LittleBoard 550 Doc & SW CD-ROM illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file in the Miscellaneous Source Code Examples subdirectory, under the LittleBoard 550 Software menu on the LittleBoard 550 Doc & SW CD-ROM.

Power Interface (J10)

The LittleBoard 550 uses five separate voltages on the board, but only one of the voltages is provided externally (+5 volts) through the external connector, which uses a 7-pin vertical header with 0.156" (3.96mm) spacing. Holes for a right angle mounting header are also available at J10. All the onboard voltages are derived from the externally supplied +5 volts DC +/- 5%. The onboard voltages provide the CPU core voltages as well as other voltages used on the board.

Table 3-27 gives the pin outs and signals for Power supply connector (J10).

Table 3-27. Power Interface Pin/Signal Descriptions (J10)

Pin #	Signal	Description
1	+5V	+5.0 volts DC +/- 5%
2	GND	Ground
3	GND	Ground
4	+12V	This +12V is are for BUS power only (optional)
5	+3.3V	This +3.3V is for BUS power only (optional)
6	GND	Ground
7	+5V	+5.0 volts DC +/- 5%

Notes: The shaded area denotes power or ground. The +12Vand +3.3V on the Power Interface connector (J10) are used for the PCI and ISA bus power and must be supplied externally. The -5V and –12V are supplied from an external power supply through the Utility 1 connector (J16).

Power Monitor

Power supply monitoring is performed by the precision triple supply monitor, LTC 1326. This chip monitors the system voltages and provides an auto-reset or external push button reset capability. The LTC 1326 monitors three separate voltages Vcore, +5V, and +3.3V. If any of these voltages drop below –10% of the nominal voltage, the POWER GOOD output is driven low causing a system reset.

CPU Fan

Table 3-28. CPU Fan (J2)

Pin #	Signal	Description
1	GND	Ground
2	+5	+5.0 volts DC +/- 5%
3	TAG	Fan Speed Tachometer

Note: The shaded area denotes power or ground.

Chapter 4 BIOS Setup

Introduction

This chapter describes the BIOS Setup menus and the various screens used for configuring the LittleBoard 550. Some features in the Operating System or application software may require configuration in the BIOS Setup screens.

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to the appropriate PC reference manuals for information about the onboard ROM-BIOS software interface. If Ampro has added to or modified the standard functions, these functions will be described.

The options provided for the LittleBoard 550 are controlled by BIOS Setup. BIOS Setup is used to configure the board, modify the fields in the Setup screens, and save the results in the onboard configuration memory. Configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and the flash memory.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted. Changes made to the Setup parameters, with the exception of the time and date settings, do not take effect until the board is rebooted.

Setup is located in the ROM BIOS and can be accessed, when prompted using the <Del> key, while the board is in the Power-On Self Test (POST) state, just before completing the boot process. The screen displays a message indicating when you can press <Del>.

The LittleBoard 550 BIOS Setup is used to configure items in the BIOS using the following menus:

- BIOS and Hardware Settings
- Reload Initial Settings
- Load Factory Default Settings
- Exit, Saving Changes
- Exit, Discarding Changes

Table 4-1 summarizes the list of BIOS menus and some of the features available for LittleBoard 550. The BIOS Setup menu offers the menu choices listed above and the related topics and screens are described on the following pages.

Accessing BIOS Setup (VGA Display)

To access BIOS Setup using a VGA display for the LittleBoard 550:

1. Turn on the VGA monitor and the power supply to the LittleBoard 550.
2. Start Setup by pressing the [Del] key, when the following message appears on the boot screen.

```
Hit <Del> if you want to run SETUP
```

NOTE	If the setting for *Memory Test* is set to Fast, you may not see this prompt appear on screen if the monitor is too slow to display it on start up. If this happens, press the <Del> key early in the boot sequence to enter BIOS Setup.

3. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.
4. Follow the instructions at the bottom of each screen to navigate through the selections and modify any settings.

Accessing BIOS Setup (Serial Console)

Entering the BIOS Setup, in serial console mode, is very similar to the steps you use to enter BIOS Setup with a VGA display, except the actual keys you use.

1. Set the serial terminal, or the PC with communications software to the following settings:
   - 115k baud
   - 8 bits
   - One stop bit
   - No parity
   - No hardware handshake
2. Connect the serial console, or the PC with serial terminal emulation, to Serial Port 1 or Serial Port 2 of the LittleBoard 550.
   - If the BIOS option, *Serial Console* is set to [Enable], use a standard null-modem serial cable.
   - If the BIOS option, *Serial Console* is set to [Hot Cable], use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
3. Turn on the serial console or the PC with serial terminal emulation and the power supply to the LittleBoard 550.
4. Start Setup by pressing the Ctl–c keys, when the following message appears on the boot screen.

```
Hit ^C if you want to run SETUP
```

5. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen. See Figure 4-1.

NOTE	The serial console port is not hardware protected, and is not listed in the COM table within BIOS Setup. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Table 4-1. BIOS Setup Menus

BIOS Setup Menu	Item/Topic
BIOS and Hardware Settings	Date and Time Drive Configuration Boot Order Drive and Boot Options Keyboard & Mouse settings User Interface options Memory settings Power management Advanced Features On-Board Features (Serial, Parallel, USB, Video, Audio, etc.) PCI and Plug and Play Options
Reload Initial Settings	Resets the BIOS (CMOS) to the most recent settings
Load Factory Default Settings	Resets BIOS (CMOS) to factory settings
Exit, Saving Changes	Writes all changes to BIOS (CMOS) and exits
Exit, Discarding Changes	Closes BIOS without saving changes except time and date

BIOS Menus

BIOS Setup Opening Screen

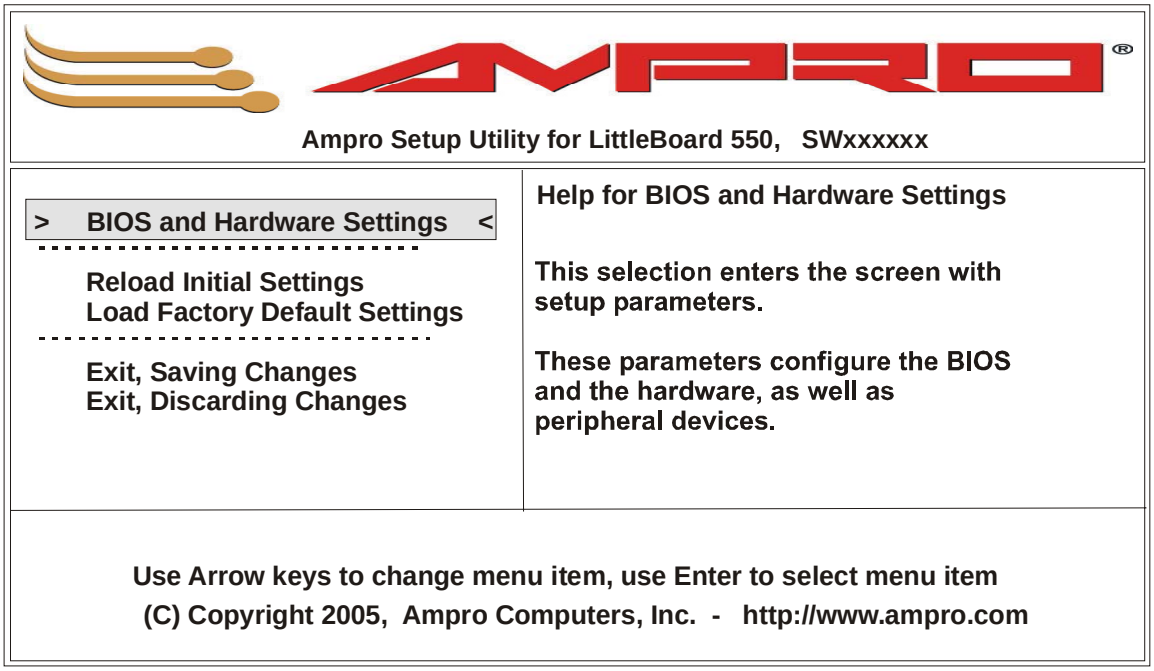


Figure 4-1. Opening BIOS Screen

NOTE	For the most current BIOS Information, refer to the Hardware Release Notes provided as hard copy in the shipping container.

NOTE	The default values or the typical settings are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the BIOS screens for navigation instructions and when making selections.

BIOS Configuration Screen

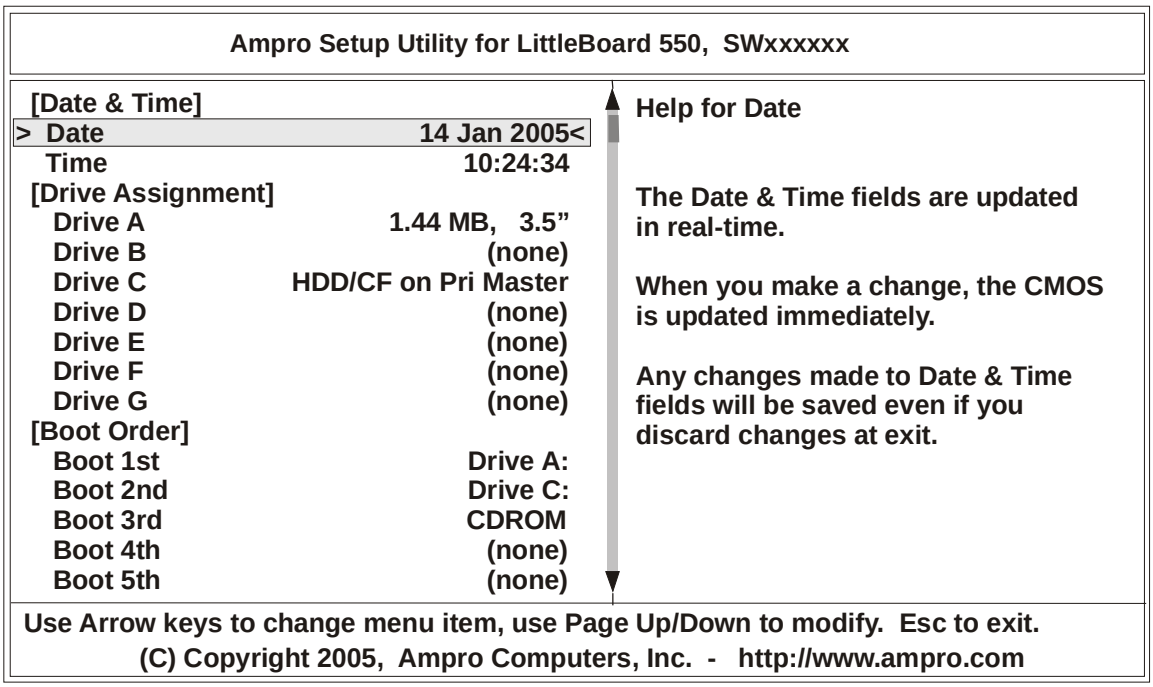


Figure 4-2. Modifying Setup Parameters Screen

- **Date & Time**
  - DATE (dd:mmm:yyyy) – This requires the alpha-numeric entry of the calendar month, day of the month, and all 4 digits of the year, indicating the century plus year (*14 Jan 2005*).
  - Time (hh:mm:ss) – This requires 24 hour Clock setting in hours, minutes, and seconds

Drive Configurations and Boot Options

Drive Assignment

- Drive A – [none], [360kB, 5.25”], [1.2MB, 5.25”], [720kB, 3.5”], [**1.44MB, 3.5”**], [2.88MB, 3.5”], or [USB Floppy]

NOTE	If USB Boot Support is [Disabled], the USB Floppy selections are invalid and Drive B must be set to [none]. See Table 4-2 Floppy Drive Setting.

- Drive B – [**none**], [360kB, 5.25”], [1.2MB, 5.25”], [720kB, 3.5”], [1.44MB, 3.5”], [2.88MB, 3.5”], or [USB Floppy]

NOTE	If an on board CompactFlash device is used in the system, it is always configured as [HDD/CF Pri Master or Slave] on Drive C or D.

- Drive C – [none], [**HDD/CF on Pri Master**], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [HDD on Sec Master], [CDROM on Sec Master], [HDD on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

NOTE	The BIOS does not support a break in the drive order, that is, Drive C can not be listed as [none] when the boot device is Drive D.

- Drive D – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [HDD on Sec Master], [CDROM on Sec Master], [HDD on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

Table 4-2. Floppy Drive BIOS Settings

# of Floppy Drive(s)	BIOS Settings
None	• Set Drives A and B to [None]
(1) Non-USB Floppy	• Configure Drive A to floppy drive type (For example, [1.44MB, 3.5”]) • Set Drive B to [None]
(1) USB Floppy	• Set USB Boot Support to [Enable] • Set Drive A to [USB Floppy] • Set Drive B to [None]
(2) Floppy drives (1 USB Floppy and 1 non-USB Floppy drive)	• Set USB Boot Support to [Enable] • Set one drive (Drive A or B) to the desired floppy drive type (For example, [1.44MB, 3.5”]) • Set the other drive (Drive B or A) to [USB Floppy]
(2) Floppy drives (2 non-USB Floppy drives)	• Set either drive (Drive A or B) to desired floppy drive type (For example, [1.44MB, 3.5”]) • Set the other drive (Drive B or A) to desired floppy drive type (For example, [1.44MB, 3.5”])

Note: A standard 34-pin floppy cable has a twist in the cable wiring between the Floppy A and B connectors, where Floppy B has the straight through cable (non-twist) and is the middle connector.

NOTE

Ampro does not recommend connecting a USB boot device to the LittleBoard 550 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 550.

Any USB (block) device that emulates a hard disk drive can be used when [USB HDD] is set as the drive option. This includes various storage media types, such as USB hard disk drives, USB CD-ROMs, CompactFlash™ cards, Secure Digital Memory Card™, and Flash or Thumb drives. Refer also to ***Boot Order*** settings**, USB Boot Support** under ***Advanced features***, and **USB** (device enable) under ***On-Board Controllers*** for USB Drive boot order, USB Boot Enable, and the number of USB ports enabled, respectively.

- Drive E – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [HDD on Sec Master], [CDROM on Sec Master], [HDD on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive F – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [HDD on Sec Master], [CDROM on Sec Master], [HDD on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]
- Drive G – [**none**], [HDD/CF on Pri Master], [CDROM on Pri Master], [HDD/CF on Pri Slave], [CDROM on Pri Slave], [HDD on Sec Master], [CDROM on Sec Master], [HDD on Sec Slave], [CDROM on Sec Slave], [USB HDD], or [USB CDROM]

- **Boot Order**
  - Boot 1st – [none], [**Drive A**], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 2nd – [none], [Drive A], [Drive B], [**Drive C**], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE	The [Alarm] option sounds beeps on the PC speaker and can be listed, like [Reboot], as the last boot device to indicate no bootable device was found. Any of the drives can be listed as a boot drive.

  - Boot 3rd – [none], [Drive A], [Drive B], [Drive C], [Drive D], [**CDROM**], [Alarm], or [Reboot]
  - Boot 4th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 5th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]
  - Boot 6th – [**none**], [Drive A], [Drive B], [Drive C], [Drive D], [CDROM], [Alarm], or [Reboot]

NOTE	The default Boot order is, A, C, D, CD-ROM, and the BIOS will start its search for a bootable device in drive A, then C, then D, then CD-ROM. If no bootable device is found, the screen will display "No Bootable Device Available" and the boot process will stop, allowing you to select from: R – for Reboot, or S – for Setup. If you do not choose R or S, the boot process stops, until you intervene, unless you have set [Reboot] as an option.

- **Drive and Boot Options**
  - Floppy Seek – [**Disabled**] or [Enabled]
  - Hard disk Seek – [**Disabled**] or [Enabled]
  - Floppy Swap – [**Disabled**] or [Enabled]
  - Boot Method – [**Boot Sector**] or [Windows CE]

    Boot Sector is the traditional method for booting the system. If [Windows CE] is selected, the BIOS attempts to load the NK.BIN file from the root directory of each boot device.
  - Primary IDE Cable – [**Auto**], [40 Wire], or [80 Wire]

    Setting these fields to [Auto], causes the BIOS to query the attached IDE device to determine the type of IDE cable used. If the BIOS detects [40 wire], or you select it, the BIOS will not use UDMA-66 or faster mode when sending signals to/from the IDE device.
  - Secondary IDE Cable – [**Auto**], [40 Wire], or [80 Wire]
  - Primary Master ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including CompactFlash cards. However, this option specifically allows you to select between the existing formats used to format your CompactFlash card as the Primary master device.
  - Primary Slave ATA mode – [**LBA**], [Physical], or [Phoenix]

    This default option (LBA - Logical Block Address) could be used on any IDE device, including CompactFlash cards. However, this option specifically allows you to select between the existing formats used to format your CompactFlash card as the Primary slave device.

NOTE	This feature allows you to use any one of the three common formats available for CompactFlash cards without having to re-format the CompactFlash card before you can use it on the LittleBoard 550. The LBA (Logical Block Address) is set as the default format because it can handle larger drives and is the newest format available, but may not be the one used to format your CompactFlash card. The other common formats that may be encountered are the Physical (below 512MB) or Phoenix (physical above 512MB) formats.

User Interface Options

- **Keyboard and Mouse** (Configuration)
  - Numlock – [**Disabled**] or [Enabled]
  - Typematic – [Disabled] or [**Enabled**]

    This field is used for the keyboard.

    - Delay – [**250ms**], [500ms], [750ms], or [1000ms]

      This field is used for the keyboard and determines how many milliseconds the keyboard controller waits before stating to repeat a key, if the key is held down on the keyboard.

    - Rate – [**30cps**], [24cps], [20cps], [15cps], [12cps], [10cps], [8cps], or [6cps]

      This is a keyboard field and determines the rate, in characters per second, the keyboard controller will repeat a key, if the key is held down on the keyboard.

  - Initialize PS/2 Mouse – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the BIOS will initialize the PS/2 mouse.

    If the PS/2 mouse is [Disabled], then the BIOS will not initialize the PS/2 mouse, which may not be recognized by the Operating System.

- **User Interface**
  - Show "Hit <Del>…" – [Disabled] or [**Enabled**]

    This field, if Enabled, will place "Hit Del" on screen during the boot process, to indicate when you may press "Del" to enter the BIOS Setup menus.

  - F1 Error Wait – [**Disabled**] or [Enabled]

    If this field is [Enabled], the BIOS will display an Error message indicating when an error has occurred during POST (power on self test) and wait for you to respond by hitting the F1 key.

    If [Disabled], and an error occurs during POST, the BIOS will attempt to continue the boot process.

  - Config Box – [Disabled] or [**Enabled**]

    This field, if Enabled, displays the Configuration Summary Box, which list all of the configuration information for the system, at the completion of POST, but before the Operating System is loaded.

  - Splash Screen – [**Disabled**] or [Enabled]

    - If Splash Screen is [Enabled] it stays on screen, until the booted Operating System changes it, if the Config Box option is Disabled.
    - If Config Box option is [Enabled], the Splash Screen stays on screen until the Config Box is displayed.

    The Splash Screen is a graphical image displayed as the default (Ampro Splash Screen) or a user customized image on screen. Refer to the Splash Screen Customization topic later in this chapter for instructions on how to customize the splash screen.

Memory Control Options

- **Memory**
  - Memory Test – [**Fast**], [Standard], or [Exhaustive]
    - If this field is set to [Fast], only basic memory tests are performed during POST to shorten POST time.
    - If this field is set to [Standard], more than basic tests are performed, but POST time is increased.
    - If this field is set to [Exhaustive], more rigorous tests are performed on memory, but this takes a significant amount of time for POST to complete.
  - Memory Hole – [**Disabled**], [1MB], or [2MB]

    This field specifies the size of an optional memory hole, below 16MB. Access to the memory addresses inside the memory hole region are forwarded to the PC/104 bus, where memory mapped PC/104 devices have access.
  - Shadow D000-D3FF – [**Disabled**] or [Enabled]

    These Shadow fields specify if BIOS option ROMs in the indicated segments should be shadowed to RAM. Shadowing option ROMs can potentially speed up the operation of the system. The indicated segments are only for option ROMs present on add-on PC/104 and PC/104-Plus cards.
  - Shadow D400-D7FF – [**Disabled**] or [Enabled]
  - Shadow D800-DBFF – [**Disabled**] or [Enabled]
  - Shadow DC00-DFFF – [**Disabled**] or [Enabled]
- **DRAM**

NOTE	The DRAM clock frequency can never be set higher than the CPU's Front Side Bus (FSB) clock frequency, regardless of the SPD or PC100 setting.

  - DRAM Clock Frequency – [**SPD**] or [PC100]

    This field specifies the DRAM clock frequency.
    - If this field is set to SPD (Serial Presence Detect), then the DRAM clock is set using the information read from the SPD(s) on the DRAM module(s).
    - If this field is set to PC100, the clock will override the DRAM SPD information and force the DRAM clock to 100MHz.
  - DRAM CAS Latency – [**SPD**], [CAS 3], or [CAS 2]

    This field specifies the DRAM CAS (Column Address Strobe) Latency
    - If this field is set to SPD, then the DRAM CAS latency is set using the information read from the SPD(s) on the DRAM module(s).
    - If this field is set to CAS 2 or CAS 3, the setting will override the DRAM SPD information and force the DRAM CAS latency to the specified value.

CAUTION	To prevent system hangs or failure at extended temperatures, do not change the DRAM Refresh Rate, Fast Precharge, and Bank Interleave values, unless you fully understand the intended results. Changing any of these settings may cause the processor to run slower or fail at extended temperatures for this board. If you change any of these settings and can not recover, use the Oops! Jumper to reset the BIOS to the defaults. The default values (DRAM Refresh Rate, Fast Precharge, and Bank Interleave) have been chosen for optimal performance and will work with the widest range of memory modules and temperatures.

- DRAM Bank Interleave – [**none**], [2], or [4]
- DRAM Fast Precharge– [**off**] or [on]
- DRAM Refresh Rate – [**4us**], [8us], or [16us]

Power Management and Advanced User Options

- **Power Management**
  - ACPI – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the Advanced Configuration and Power Interface API is turned on.
  - APM – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Advanced Power Management API is turned on.
- **Advanced features**
  - Post Memory Manager – [**Disabled**] or [Enabled]

    If this field is set to [Enabled], the Post Memory Manger API is turned on. The Post Memory Manger can be used by BIOS option ROMs to allocate memory for optimal performance.
  - CPU Serial Number – [**Disabled**]

    This field is inoperable since the VIA Eden ESP CPUs do not have a unique internal serial number, which can be accessed by the BIOS or an Operating System/Application.
  - Watchdog Timeout (sec) – [select whole number between 1 and 255 seconds, in 1 second increments] or [**Disabled**]

    If this field is enabled by selecting a time interval (1 to 255 seconds), will direct the watchdog timer to reset the system if it fails to boot the OS properly. Refer to the watchdog timer section in Chapter 3 for more information.
  - Serial Console – [**Hot Cable**] or [Enabled]
    - The Hot Cable option only allows console redirection when a Hot Cable is actually connected to COM 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.
    - The [Enabled] option instructs the BIOS to operate in the console redirection mode at all times with the serial port selected in the Serial Console > Port field listed below. Use a standard null-modem serial cable.
    - However, connecting a Hot Cable to the other port (port not selected) overrides the setting of this field [Enabled] and the Serial Console > Port field.

    - Port – [**3F8h**], [2F8h], [3E8h], or [2E8h]

      This field selects the COM (Serial) port address used for console redirection when [Enabled] has been selected in Serial Console. Use a standard null-modem serial cable.

However, connecting a Hot Cable to the other port (port not selected) overrides this field setting and activates the connected port. Connecting a Hot Cable to one of the serial ports only allows console redirection when a Hot Cable is actually connected to Serial 1 or 2. Use the modified serial cable described in Chapter 3, under *Hot (Serial) Cable*.

♦ USB Boot Support – [**Disabled**] or [Enabled]

This field allows you to select any USB device as a boot device. Refer also *to **Drive Assignment*** settings, ***Boot Order*** settings, and **USB** (device enable) under ***On-Board Controllers*** for the USB Drive settings and the number of USB ports enabled, respectively.

- If this field is set to [Disabled], none of the USB devices connected to the LittleBoard 550 can be used as a boot device.
- If this field is set to [Enabled], any of the bootable USB devices connected to the LittleBoard 550 can be used as a boot device.

NOTE	Ampro does not recommend connecting a USB boot device to the LittleBoard 550 through an external hub. Instead, connect the USB boot device directly to the LittleBoard 550.

♦ LAN Boot – [**None**], [LAN 1], or [LAN 2]

This field allows you to boot the system over one of the Ethernet connections (LAN). Refer to the topics, **LAN Boot** and **PXE Agent BIOS Settings,** in Appendix C, *LAN Boot Option* for more information.

NOTE	LAN Boot is an option and only appears in the BIOS Setup Utility if you have had a BIOS update installed by Ampro, to make use of the LAN Boot option.

- If this field is set to [LAN 1], the LittleBoard 550 will boot from Ethernet 1 (J7). If you enable LAN Boot for [LAN 1], you will need to saves changes, reboot the system, and go to the PXE Agent BIOS settings. Refer to Appendix C, for more information.
- If this field is set to [LAN 2], the LittleBoard 550 will boot from Ethernet 2 (J32). If you enable LAN Boot for [LAN 2], you will need to saves changes, reboot the system, and go to the PXE agent BIOS settings. Refer to Appendix C, for more information.

- **On-Board Serial Ports**

NOTE	Serial Ports 1 and 2 can not share the same IRQs, and the IRQs used for Serial Ports 1 and 2 can not be used for Serial Ports 3 and 4 and vice versa.

♦ Serial 1 – [Disabled], [**3F8h**], [2F8h], [3E8h], [2E8h], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

This field specifies the base address used for Serial Port 1.

- IRQ – [none], [1], [3], [**4**], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

  This field specifies the IRQ used for Serial Port 1. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Mode – [**RS-232**] or [RS-485]

  This field specifies the signal mode, RS232, or RS485, used for Serial Port 1. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

♦ Serial 2 – [Disabled], [3F8h], [**2F8h**], [3E8h], [2E8h], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

This field specifies the base address used for Serial Port 2.

- IRQ – [none], [1], [**3**], [4], [5], [6], [7], [9], [10], [11], [12], [14], or [15]

  This field specifies the IRQ used for Serial Port 2. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Mode – [**RS-232**] or [RS-485]

  This field specifies the signal mode, RS232, or RS485, used for Serial Port 2. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

♦ Serial 3 – [Disabled], [3F8h], [2F8h], [**3E8h**], [2E8h], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

This field specifies the base address used for Serial Port 3.

- IRQ – [3], [4], [5], [7], [9], [10], or [**11**]

  This field specifies the IRQ used for Serial Port 3. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Mode – [**RS-232**] or [RS-485]

  This field specifies the signal mode, RS232, or RS485, used for Serial Port 3. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

♦ Serial 4 – [Disabled], [3F8h], [2F8h], [3E8h], [**2E8h**], [260h], [2F0h], [3E0h], [2E0h], [200h], or [220h]

This field specifies the base address used for Serial Port 4.

- IRQ – [3], [4], [5], [7], [9], [**10**], or [11]

  This field specifies the IRQ used for Serial Port 4. If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- Mode – [**RS-232**] or [RS-485]

  This field specifies the signal mode, RS232, or RS485, used for Serial Port 4. If [RS-485] mode is selected, the RTS signal should be used to control the direction for this port (transmit or receive).

- **On-Board LPT Port**

♦ LPT 1 – [Disabled], [**378h**], [278h], [3BCh], [370h], or [270h]

This field specifies the base address used for the parallel port (LPT 1).

- IRQ – [none], [1], [3], [4], [5], [6], [**7**], [9], [10], [11], [12], [14], or [15]

  This field specifies the IRQ used for the parallel port (LPT 1). If this field is set to [none], then no IRQ is assigned, making it available for other devices.

- DMA – [**3**], [2], [1], or [0]

  This field specifies the DMA channel used for the parallel port (LPT 1). If the LPT 1 field is set to [Disabled], then no DMA channel is assigned, making it available for other devices.

- Mode – [**Standard**], [SPP (bi-dir)], [EPP 1.9 + SPP], [EPP 1.7 + ECP], [EPP 1.9 + ECP], or [ECP]

  This field specifies the Mode used for the parallel port (LPT1).

- **On-Board Controllers**

  - Floppy – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Floppy controller is used.

  - Primary IDE – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Primary IDE controller is used.

  - Secondary IDE – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], then the on-board Secondary IDE controller is used.

  - PS/2 Mouse – [Disabled] or [**Enabled**]

    - If this field is set to [Enabled], then the on-board PS/2 Mouse controller is used and assigned an IRQ by the BIOS, typically IRQ 12.
    - If this field is set to [Disabled], then the on-board PS/2 Mouse controller is not used and IRQ 12 is available for other devices.

  - USB – [Disabled], [2 Ports] or [**4 Ports**]

    - If this field is set to [4 Ports], both on-board USB controllers are used, each one supporting two USB ports.
    - If this field is set to [2 Ports], the first on-board USB controller is used, supporting two USB ports, and the second on-board USB controller is disabled.

  - Audio – [Disabled] or [**Enabled**]

    If this field is set to [Enabled], the on-board Audio controller is used.

Video, Flat Panel, and Audio Options

- **On-Board Video**

  - Framebuffer Size – [Disabled], [**8MB**], [16MB], or [32MB]

    This field specifies the amount of system memory used for the on-board Video Framebuffer. The amount of memory used for the Framebuffer of the on-board Video controller is subtracted from the available system memory.

  - AGP Aperture Size – [2MB], [4MB], [8MB], [16MB], [32MB], [64MB], [**128MB**], or [256MB]

    This field specifies the size of memory used for the AGP Aperture. The AGP Aperture Size indicates the amount of system memory that can be used for the 3D engine. The system memory is still available for the system use, unless an application actually uses the AGP Aperture memory.

  - Display – [**CRT**], [LCD], [LCD + CRT]

    This field specifies the display type used.

    - If [LCD] or [CRT+LCD] is selected, the panel type selection indicates the configuration of the LCD panel attached. See the Panel Type field and Table 4-2.

- If the [CRT+LCD] is selected, the same video information is shown on both displays simultaneously.

♦ Panel Type – [**640 x 480 x 18 TFT**]

Refer to Table 4-3 for the list of supported resolutions and flat panel types and the Software Release Notes for the signal pin assignments. Some LCD panels may require video BIOS modifications. If you would like help in setting up your LCD panel, contact Virtual Technician on the web site for assistance with the LCD panel adaptation.

Table 4-3. LCD Panel Type List

#	LCD Resolution	LCD Type
1	**640 x 480 x 18 (bit)**	**TFT**
2	800 x 600 x 18 (bit)	TFT*
3	1024 x 768 x 18 (bit)	TFTx2
4	1280 x 1024 x 18 (bit)	TFTx2
5	640 x 480 x 16 (bit)	DSTN
6	800 x 600 x 16 (bit)	DSTN*
7	1600 x 1200 x 18 (bit)	TFTx2
8	1024 x 768 x 18 (bit)	TFT*

#	LCD Resolution	LCD Type
9	640 x 480 x 18 (bit)	TFT*
10	800 x 600 x 18 (bit)	TFT
11	1024 x 768 x 18 (bit)	TFT
12	1280 x 1024 x 18 (bit)	TFT
13	1400 x 1050 x 18 (bit)	TFTx2
14	800 x 600 x 16 (bit)	DSTN*
15	1024 x 768 x 16 (bit)	DSTN
16	1280 x 1024 x 16 (bit)	DSTN

- **On-Board Audio Legacy**

♦ SoundBlaster – [**Disabled**], [220-22Fh], [240-24Fh], [260-26Fh], or [280-28Fh]

This field indicates the base address of the on-board Audio controller used to emulate the SoundBlaster, or is disabled.

- IRQ – [**5**], [7], [9], or [10]

  If the SoundBlaster emulation is [Disabled], then no IRQ is used.

- DMA – [3], [2], [**1**], or [0]

  If the SoundBlaster emulation is [Disabled], then no DMA channel is used.

♦ MPU 401 Midi – [**Disabled**], [300-303h], [310-313h], [320-323h], or [330-333h]

This field indicates the base address of the on-board Audio controller used to emulate MPU-401 Midi, or is disabled.

PCI, Plug n' Play, and Interrupt Assignments

- **PCI**

♦ INTA IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]

♦ INTB IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]

♦ INTC IRQ – [none], [1], [3], [4], [**5**], [6], [7], [9], [10], [11], [12], [14], or [15]

♦ INTD IRQ – [none], [1], [3], [4], [5], [6], [7], [**9**], [10], [11], [12], [14], or [15]

- **Plug and Play**

♦ PnP BIOS – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], the BIOS uses Plug and Play adapter initialization and assigns the resources, such as I/O addresses, IRQs, and DMA channels to Plug and Play compatible devices. The resources assigned by the BIOS are based on the settings of the IRQ and DMA channel assignments listed in the following fields.

- If this field is set to [Disabled], the IRQs and DMA channels listed below can not be assigned to Plug and Play devices.

♦ PnP OS – [Disabled] or [**Enabled**]

If this field is set to [Enabled], the BIOS makes the Plug and Play API available for Plug and Play Operating Systems. This allows the Plug and Play OS to get the Plug and Play information by calling the Plug and Play API.

♦ Assign IRQ 1 – [**Disabled**] or [Enabled]

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 3 – [Disabled] or [**Enabled**] (Typically COM2)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 4 – [Disabled] or [**Enabled**] (Typically COM1)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 5 – [Disabled] or [**Enabled**]

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 6 – [**Disabled**] or [Enabled] (Typically Floppy Disk)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 7 – [Disabled] or [**Enabled**] (Typically LPT1)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

♦ Assign IRQ 9 – [Disabled] or [**Enabled**] (Typically unused)

- If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
- If another device in the system is using this IRQ, then this field should be set to [Disabled].

- Assign IRQ 10 – [Disabled] or [**Enabled**] (Typically unused)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 11 – [Disabled] or [**Enabled**] (Typically ISA Bridge/Native IDE)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 12 – [**Disabled**] or [Enabled] (Typically PS/2 Mouse)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 14 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign IRQ 15 – [**Disabled**] or [Enabled] (Typically Hard Disk)
  - If this field is set to [Enabled], then the BIOS can assign this IRQ to a Plug and Play adapter.
  - If another device in the system is using this IRQ, then this field should be set to [Disabled].
- Assign DMA 0 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 1 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 2 – [**Disabled**] or [Enabled]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].

- Assign DMA 3 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 5 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 6 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].
- Assign DMA 7 – [Disabled] or [**Enabled**]
  - If this field is set to [Enabled], then the BIOS can assign this DMA channel to a Plug and Play adapter.
  - If another device in the system is using this DMA channel, then this field should be set to [Disabled].

Splash Screen Customization

The LittleBoard 550 BIOS supports a graphical splash screen, which can be customized by the user and displayed on screen when enabled through the BIOS Setup Utility. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image displayed on screen during the boot process and remain there, depending on the options selected in BIOS Setup, while the OS boots.

Splash Screen Image Requirements

The user's image may be customized with any bitmap software editing tool, but must be converted into an acceptable format with the tools (files and utilities) provided by Ampro. If the custom image is not converted with the utilities provided, then the image will not display properly when this field is selected in BIOS Setup.

NOTE	Do not use other splash screen conversion tools, as these will render an image that is not compatible with the LittleBoard 550 BIOS.

The splash screen image supported by the LittleBoard 550 BIOS should be:

- Bitmap image
- Exactly 640x480 pixels
- Exactly 16 colors
- A converted file size of not greater than 55kB

Converting the Splash Screen File

The following files are provided by Ampro on the LittleBoard 550 Doc & SW CD-ROM and are required for converting a custom splash screen file. Refer to the CD-ROM for the utilities and an example of how to load a custom image in the *lb550\software\examples\splash* directory.

- splash.bmp
- convert.exe
- convert.idf
- resplash.com
- lb550.bin

The process of converting and loading a custom image onto the LittleBoard 550 involves the following sequence of events:

- Prepare directory for conversion (create directory and copy files into it)
- Obtain the LittleBoard 550 BIOS binary
- Prepare the custom image file
- Convert the image to an acceptable BIOS format
- Merge the image with BIOS binary to create new BIOS binary
- Load the new BIOS binary onto the LittleBoard 550

NOTE	You can use any Windows PC to convert the custom image, but your PC must have an internet browser to access, view, and make selections in the main menu of the LittleBoard 550 Doc & SW CD-ROM. For example: Microsoft Internet Explorer 4.x, or greater, Netscape Navigator version 4.x, or greater, or the equivalent.

Use the following steps to convert and load your custom image onto the LittleBoard 550.

1. Copy the files from the *LB550\software\examples\splash* directory on the CD-ROM to a new directory (conversion directory) on your PC.

   This new conversion directory is where you intend to do the conversion and save the file.

2. Remove the read-only attributes from all the files as part of the file copying process.

3. Copy the LittleBoard 550 BIOS binary file (lb550.bin) to the new conversion directory on your PC where the other files and utilities are located.

   If this file is not on the LittleBoard 550 Doc & SW CD-ROM, you will have to obtain it from Ampro.

NOTE	Ampro recommends keeping a copy of this original lb550.bin file, just in case you encounter problems with your new file or have difficulty updating the BIOS with the new image.

4. Prepare your custom image file with any Windows bitmap software editing tool.

   - For example, Corel Photo-Paint, Adobe Photoshop, or the Windows Paint program provided with Windows. You can insert a desired graphic image, logo, text, etc. into the file.
   - The custom image must be a bitmap image in .bmp format at 640x480 pixels and it must be 16 colors. The file should be about 153,718 bytes. Refer to the example file splash.bmp.

5. Save your custom image file as splash.bmp at 640x480 pixels by 16 colors.

   - If your custom image file is not approximately 153,718 bytes in size it is probably not in the right format or is too complex to be used in the BIOS. You will have to edit it down in size until you have reached an acceptable file size.
   - If you are doubtful about the conversion process, due to the file size, Ampro recommends making a copy of your new splash.bmp, so that you can edit it later if the conversion does not yield a small enough file. Otherwise, you may have to re-create your custom image before you can edit it down to an acceptable file size.

6. If your custom image file is not on the conversion PC, copy the new splash.bmp file to the conversion directory.

7. Run the following command from DOS, or a Windows DOS pop-up screen to convert your new splash.bmp file.

   ```
   C:\splash>convert convert.idf
   ```

   This conversion should yield a *splash.rle* file of approximately 55kB in size or less, depending on the complexity of your image.

8. If the splash.rle file size is greater than 55kB, go back to the unconverted image file and edit the file.

   You may reduce the file size of the converted image (splash.rle) by reducing the image's complexity.

9. Run the following command to merge the converted image with the BIOS binary file.

   ```
   C:\splash>resplash lb550.bin splash.rle lb550n.bin
   ```

   This creates a new BIOS named lb550n.bin, which has the new splash image. This new BIOS is ready to be loaded onto the LittleBoard 550.

10. Copy the files update.bat, aflash.exe, and lb550n.bin to a DOS boot floppy.

11. Boot the LittleBoard 550 from the floppy and run update.bat.

12. Cycle the power to the LittleBoard 550 and enter BIOS Setup to enable the splash screen.

Appendix A Technical Support

Ampro Computers, Inc. provides a number of methods for contacting Technical Support listed in the Table A-1 below. Requests for support through the Virtual Technician are given the highest priority, and usually will be addressed within one working day.

- Ampro Virtual Technician – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro web site at http://ampro.custhelp.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online before you can log in to access this service.
- Personal Assistance – You may also request personal assistance by going to the "Ask a Question" area in the Virtual Technician. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request you can go to the "My Stuff" area and log in to check status, update your request, and access other features.
- Embedded Design Resource Center – This service is also free and available 24 hours a day at the Ampro web site at http://www.ampro.com. However, you must be registered online before you can log in to access this service.

  The Embedded Design Resource Center was created as a resource for embedded system developers to share Ampro's knowledge, insight, and expertise gained from years of experience. This page contains links to White Papers, Specifications, and additional technical information.

Table A-1. USA Technical Support Contact Information

Method	Contact Information
Virtual Technician	http://ampro.custhelp.com
Web Site	http://www.ampro.com
Standard Mail	Ampro Computers, Incorporated 5215 Hellyer Avenue San Jose, CA 95138-1007, USA

Appendix B Connector Part Numbers

The following table provides the connector part numbers, or the equivalent, and if applicable the ribbon-cable part number, used as the mating connector to the referenced connectors on the LittleBoard 550. All connectors use 0.100" (2.54mm) pin spacing unless otherwise indicated.

Table B-1. Connector and Manufacturers' Part Numbers

Connector	Designation	Pin #	Mfg	Part Number
J2	Fan	3-pin	Molex	Housing 22-01-2037 Pins 08-50-0114 (discrete wires)
J10	Power In	7-pin, 0.156"/3.96mm	Molex AMP	Housing 09-50-8073 Housing 770849-7
			Molex AMP	Pins 08-52-0071 (discrete wires) Pins 350980 (discrete wires)
J5, J18	Video (CRT), Utility 3	10-pin	MMT PHYCO	Housing IDCA001-F0502GFT Housing 1100-10NP
			Belden	Flat Cable 9L28010
J4, J16	Video (LCD 2), Utility 1	16-pin	MMT PHYCO	Housing IDCA001-F0802GFT-K Housing 1100-16
			Belden	Flat Cable 9L28016
J11, J13	Serial A & B	20-pin	MMT PHYCO	Housing IDCA001-F1002GFT-K Housing 1100-20
			Belden	9L28020
J31	Video (LVDS)	20-pin, 1.25mm	Molex	Housing 51127-2005 Pins 50516-8041 (discrete wires)
J24	Utility 2	24-pin	3M Amphenol	Housing 3626-6600 Housing 812-1633-1118H
			Belden	Flat Cable 9L28024
J15	Parallel	26-pin	MMT PHYCO	Housing IDCA001-F1302GFT Housing 1100-26NP
			Belden	Flat Cable 9L28025
J28	Audio In/Out	26-pin, 2mm	MMT FCI	Housing IDCB-F1302GFT Housing 89947-126
			Belden	Flat Cable 2L28016
J14	Floppy	34-pin	AMP PHYCO	Housing 746285-8 Housing 1100-34NP
			Belden	Flat Cable 9L28034
			Molex Samtec	Key Plug 15-04-0292 Key Plug PK-01
J12, J17	Primary & Secondary IDE	40-pin	3M	Housing 3417-7040
			Belden	Flat Cable 9L28040
			3M	Key Plug 3435-0
J3	Video (LCD 1)	50-pin	3M	Housing 3425-7050
			Belden	Flat Cable 9L28050

Appendix C LAN Boot Option

The LAN Boot feature is optional for the LittleBoard 550 and you must contact Ampro or your sales representative for more information before you can make use of this option. The LAN Boot option requires a BIOS update to make use of the LAN Boot features.

Introduction

LAN Boot is supported by both Ethernet ports on the LittleBoard 550, and is based on the Preboot Execution Environment (PXE), an open industry standard. PXE (pronounced “pixie”) was designed by Intel, along with other hardware and software vendors, as part of the Wired for Management (WfM) specification to improve management of desktop systems. This technology can also be applied to the embedded system market place. PXE turns the LittleBoard 550 Ethernet ports into boot devices when connected over a network (LAN).

PXE boots the LittleBoard 550 from the network (LAN) by transferring a "boot image file" from a server. This image file is typically the operating system for the LittleBoard 550, or a pre-OS agent that can perform management tasks prior to loading the image file (OS). A management task could include scanning the hard drive for viruses before loading the image file.

PXE is not operating system-specific, so the image file can load any OS. The most common application of PXE (LAN Boot) is installing an OS on a brand new device (hard disk drive) that has no operating system, (or reinstalling it when the operating system has failed or critical files have been corrupted).

Using PXE prevents the user from having to manually install all of the required software on the storage media device, (typically a hard disk drive) including the OS, which might include a stack of installation CD-ROMs. Installing from the network is as simple as connecting the ReadyBoard to the network and powering it on. The server can be set up to detect new devices and install software automatically, thereby greatly simplifying the management of small to large numbers of systems attached to a network.

If the hard disk drive should crash, the network can be set up to do a hardware diagnostic check, and once a software-related problem is detected, the server can re-install the defective software, or all the ReadyBoard software from the server. Booting from the network also guarantees a "clean" boot, with no boot-time viruses or user-modified files. The boot files are stored on the PXE server, protected from infection and user-modification.

To effectively make use of the Ampro supplied feature (LAN Boot), the LittleBoard 550 requires a PXE boot agent for set up and PXE components on the server side as well. These include a PXE server and TFTP (Trivial File Transfer Protocol) server. The PXE server is designed to work in conjunction with a Dynamic Host Configuration Protocol (DHCP) server. The PXE server can be shared with DHCP server or installed on a different server. This makes it possible to add PXE to an existing network without affecting the existing DHCP server or configuration. Refer to the web sites listed here for sources of PXE boot agents and server components. For a more detailed technical description of how PXE works go to, http://www.pxe.ca. For more detailed information concerning pre-OS agents, go to: http://www.pre-OS.com.

Ampro provides a third party PXE boot agent integrated into the LittleBoard 550 BIOS when you get the BIOS upgrade, but does not provide the PXE server components. You will also need to provide your own PXE server components on a compatible PXE server, before making full use of the LAN Boot feature. The BIOS upgrade for the LittleBoard 550 has the LAN Boot options avaiable for selection. When you change the BIOS settings to enable LAN Boot, you will need to exit BIOS Setup, saving your settings, and reboot the system to enter and set the PXE boot agent settings. Refer to the topic *BIOS Setup* and Appendix C, *PXE Boot Agent BIOS Setup* for more information and configuration information.

PXE Boot Agent BIOS Setup

This section describes the BIOS settings of the third party PXE Boot agent provided by Ampro and integrated into the LittleBoard 550 firmware upgrade. The PXE Boot Agent's BIOS setup menu and screens are used when configuring the LAN boot feature in the LittleBoard 550 BIOS.

The third party PXE Boot agent provided by Ampro supports multiple boot protocols and network environments such as traditional TCP/IP, NetWare, and RPL. It also includes support for all of the most used protocols including DHCP, BOOTP, RPL, NCP/IPX (802.2, 802.3, Ethernet II), and the Wired for Management (WfM) 2.0 specification for Preboot Execution Environment (PXE).

Accessing PXE Boot Agent BIOS Setup

To access PXE Boot Agent BIOS Setup when LAN Boot has been selected in the LittleBoard 550 BIOS Setup screen, refer to this procedure:

1. Reboot the LittleBoard 550 after selecting LAN 1 or LAN 2 in BIOS Setup.

   The default setting for LAN boot is [None].

2. Access the LAN Boot Setup by pressing the Ctrl +Alt + B keys, when the following message appears on the boot screen.

   ```
   Initializing MBA.  Press Ctrl + Alt + B to configure ..
   ```

3. Select from the menu options when the default screen appears as shown in Figure C-1.
4. Follow the instructions at the bottom of the screen to navigate through the selections and modify any settings.

NOTE	The default values are shown highlighted (**bold text**) in the list of options on the following pages. Refer to the bottom of the Setup screen for navigation instructions and when making selections.

PXE Boot Agent Setup Screen

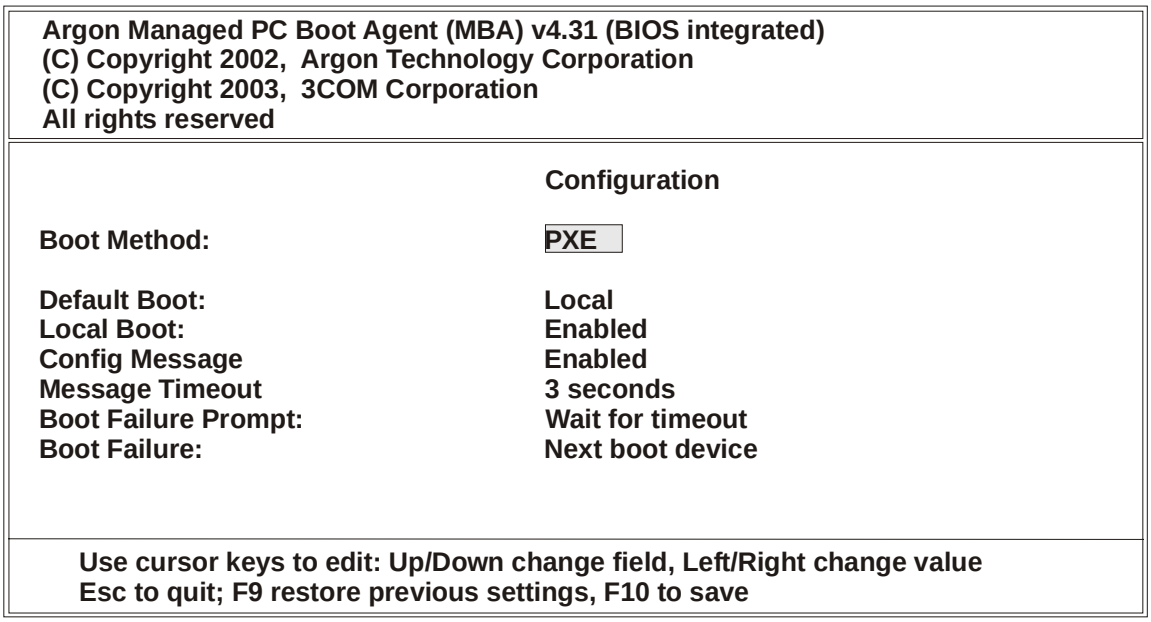


Figure B-1. PXE Agent Boot Setup Screen

- **PXE Configuration**
  - Boot Method: – [**PXE**], [TCP/IP], [NetWare], or [RPL]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **TCP/IP Configuration**
  - Boot Method: – [PXE], [**TCP/IP**], [NetWare], or [RPL]
  - Protocol: – [**DHCP**] or [BOOTP]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **NetWare Configuration**
  - Boot Method: – [PXE], [TCP/IP], [**NetWare**], or [RPL]
  - Protocol: – [802.2], [**802.3**], or [EthII]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

- **RPL Configuration**
  - Boot Method: – [PXE], [TCP/IP], [NetWare], or [**RPL**]
  - Default Boot: – [**Local**] or [Network]
  - Local Boot: – [Disabled] or [**Enabled**]
  - Config Message: – [Disabled] or [**Enabled**]
  - Message Timeout: – [**3 seconds**], [6 seconds], [12 seconds], or [Forever]
  - Boot Failure Prompt: – [**Wait for timeout**] or [Wait for key]
  - Boot Failure: – [**Next boot device**] or [Reboot]

Index